Error Correction Coding for Flash Memories

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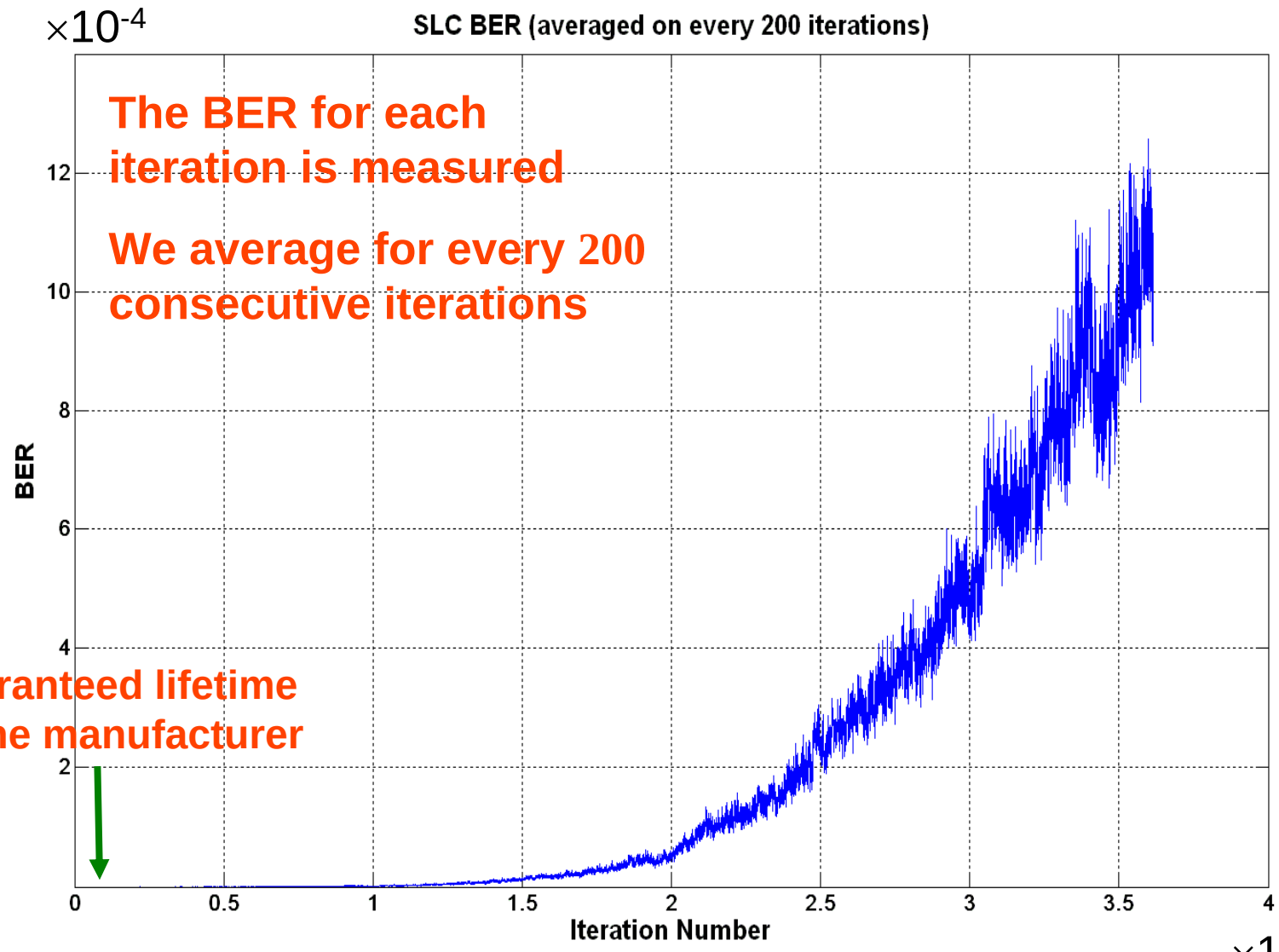
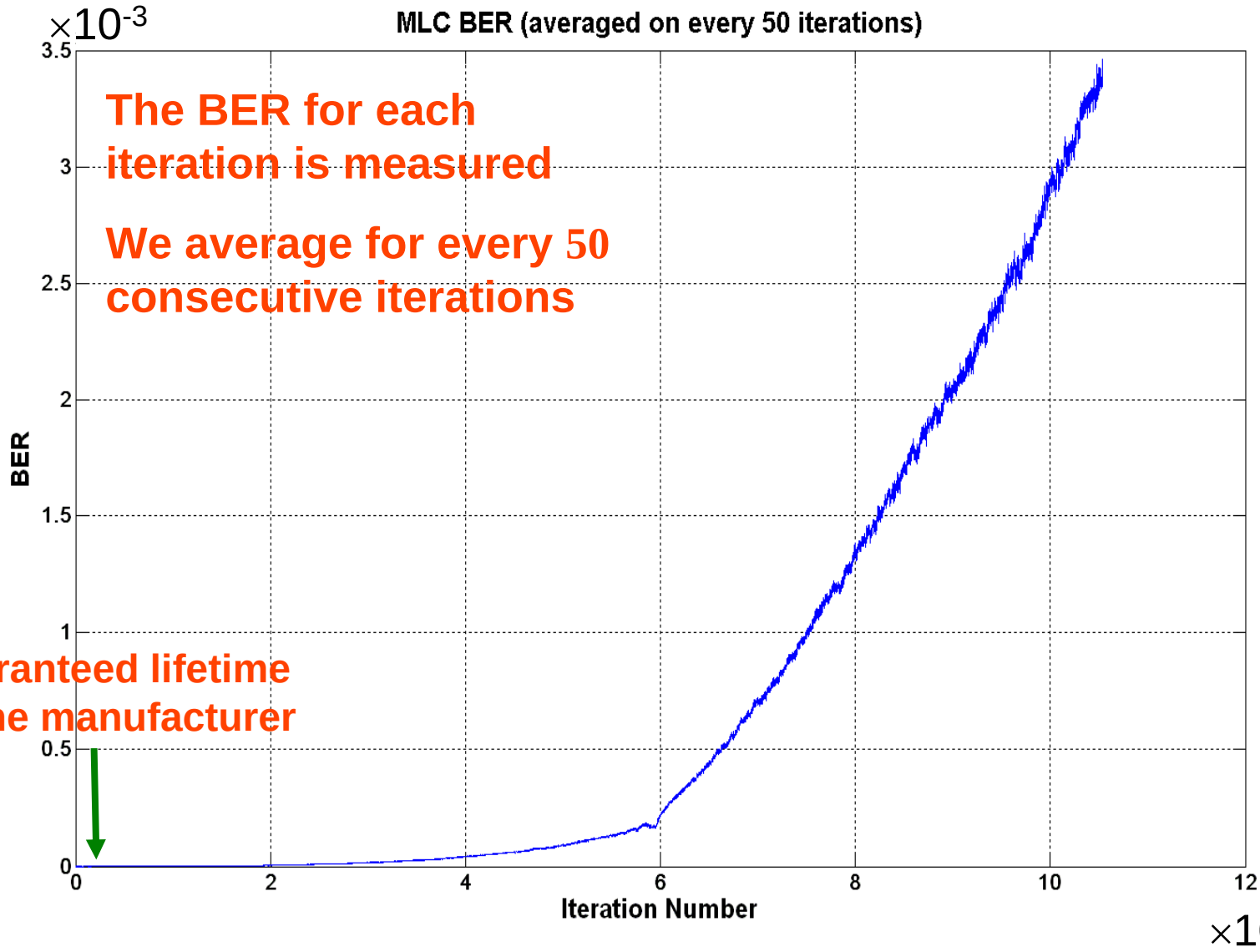
Experiment Description

- We checked several flash memory blocks - **SLC** and **MLC**
- For each block the following steps are repeated
  - The block is **erased**
  - A pseudo-random data is **written** to the block
  - The data is **read** and **compared** to find errors
- Two runs are chosen as representatives for SLC and MLC
  - **SLC** - Collected Iterations: **3,615,224**
  - **MLC** - Collected Iterations: **1,054,031**
- **Remarks**:
  - We measured many more iterations than the manufacturer's guaranteed number of erasures
  - The experiment was done in a lab conditions and related factors such as temperature change, intervals between erasures or multiple readings before erasures were not considered

Raw BER for SLC block



Raw BER for MLC block



Basic Error Characteristic

- **Directional Errors** - Number of Plus errors Vs. Minus errors
  - **Plus error**: Cell in state **'0'** changes to state **'1'**
  - **Minus error**: Cell in state **'1'** changes to state **'0'**
  - We check the distribution of the errors between plus and minus errors and the numbers are the same even for individual bits
  - **Conclusion**: There is no preference to correct more plus than minus errors (or vice versa)
- **Burst behavior**
  - Check how close the errors are to each other
  - Explore the potential (dis)advantage of using a RS code VS a BCH code
  - **Conclusion**: The errors are random and do not have burst pattern behavior

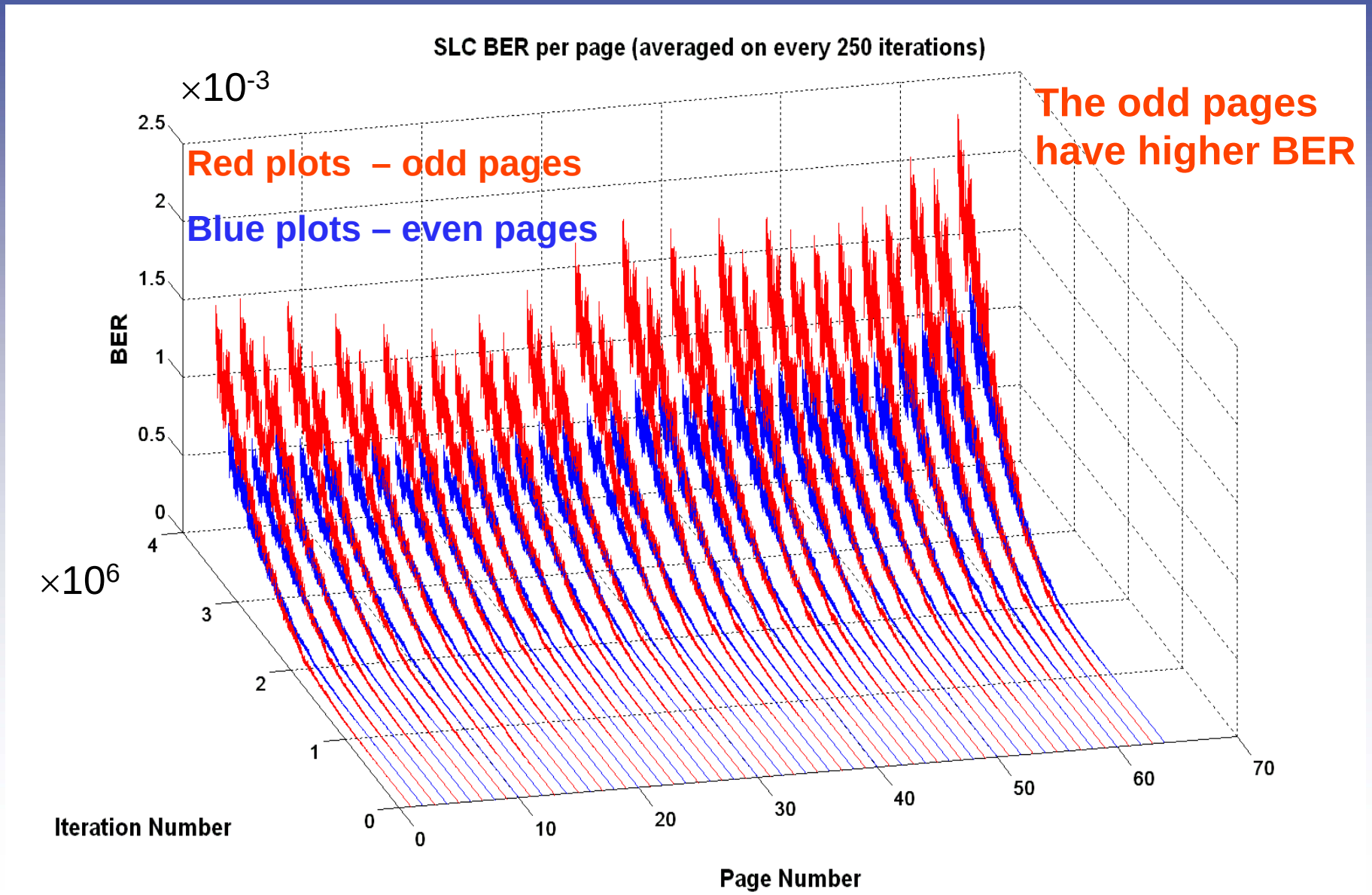
SLC - BER Page Dependency

- We checked the BER for each page **independently**
- SLC block cells layout:

  $32x2^{15}$ cells; each page has 2^{14} cells

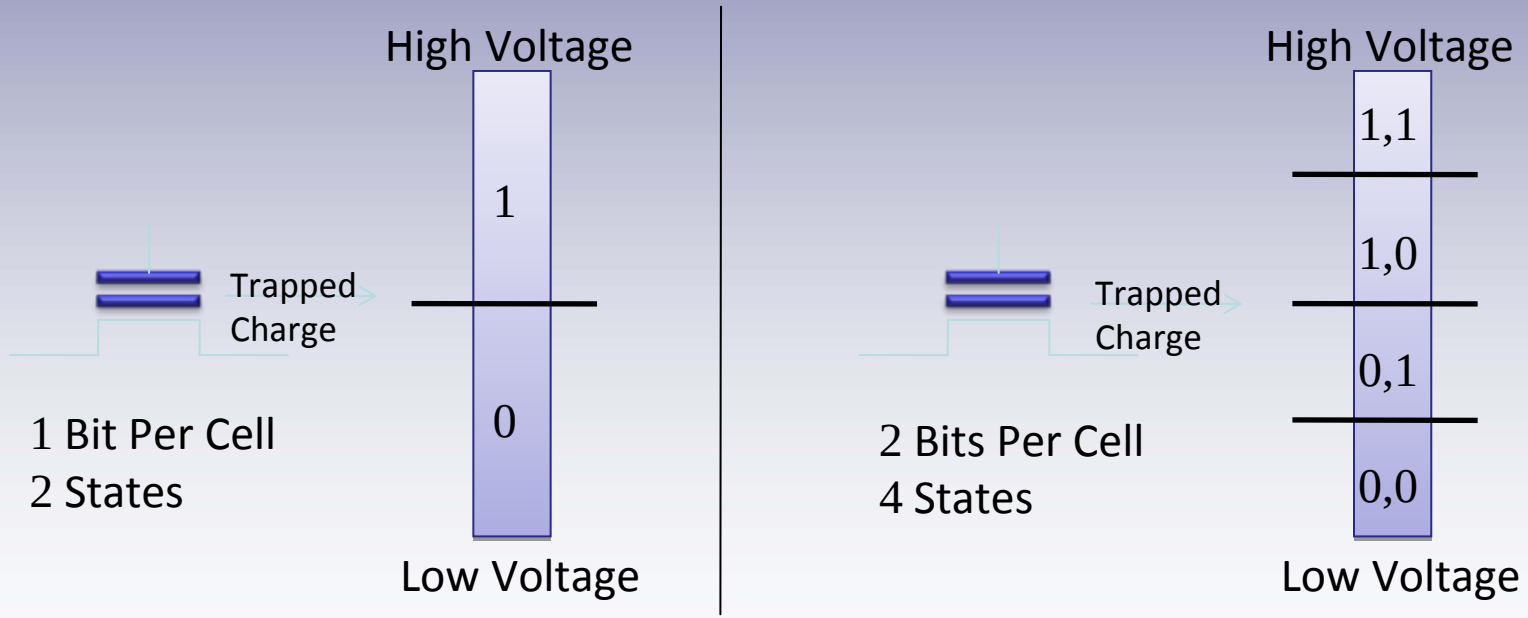
page 1	page 2
page 3	page 4
page 5	page 6
.	.
.	.
.	.
page 63	page 64

SLC - BER Page Dependency



MLC - BER Page Dependency

- The Most Significant Bit (**MSB**) and Least Significant Bit (**LSB**) represented by one cell belong to two different pages
- Pages storing the LSB are less protected from errors



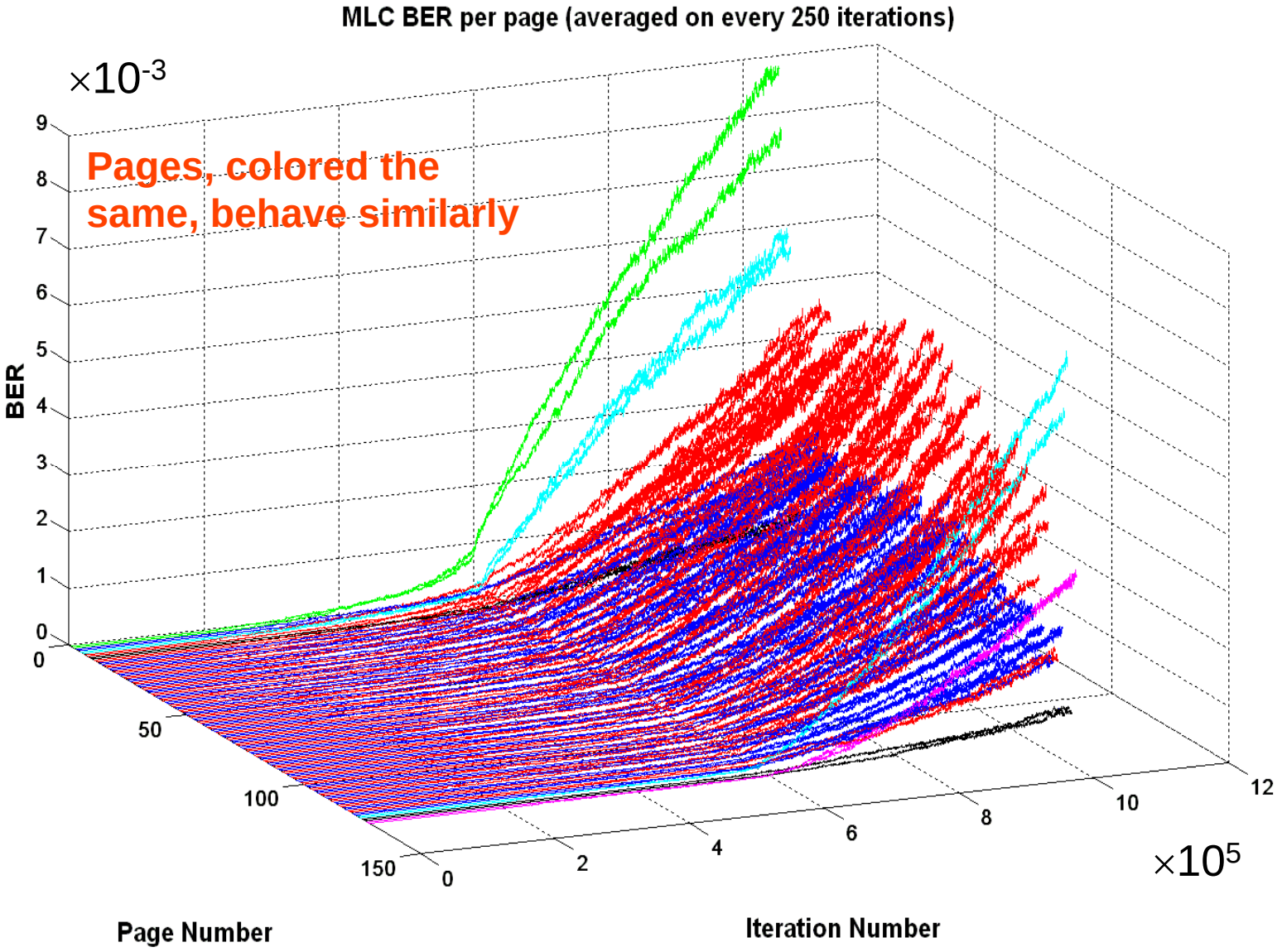
Single Level Cell (SLC) **Multi Level Cell (MLC)**

MLC - BER Page Dependency

A possible MLC block cell layout:

Row index	**LSB** of **first** 2^{14} cells	**MSB** of **first** 2^{14} cells	**LSB** of **last** 2^{14} cells	**MSB** of **last** 2^{14} cells
1	page 1	page 5	page 2	page 6
2	page 3	page 9	page 4	page 10
3	page 7	page 13	page 8	page 14
4	page 11	page 17	page 12	page 18
5	page 15	page 21	page 16	page 22
M	M	M	M	M
31	page 119	page 125	page 120	page 126
32	page 123	page 127	page 124	page 128

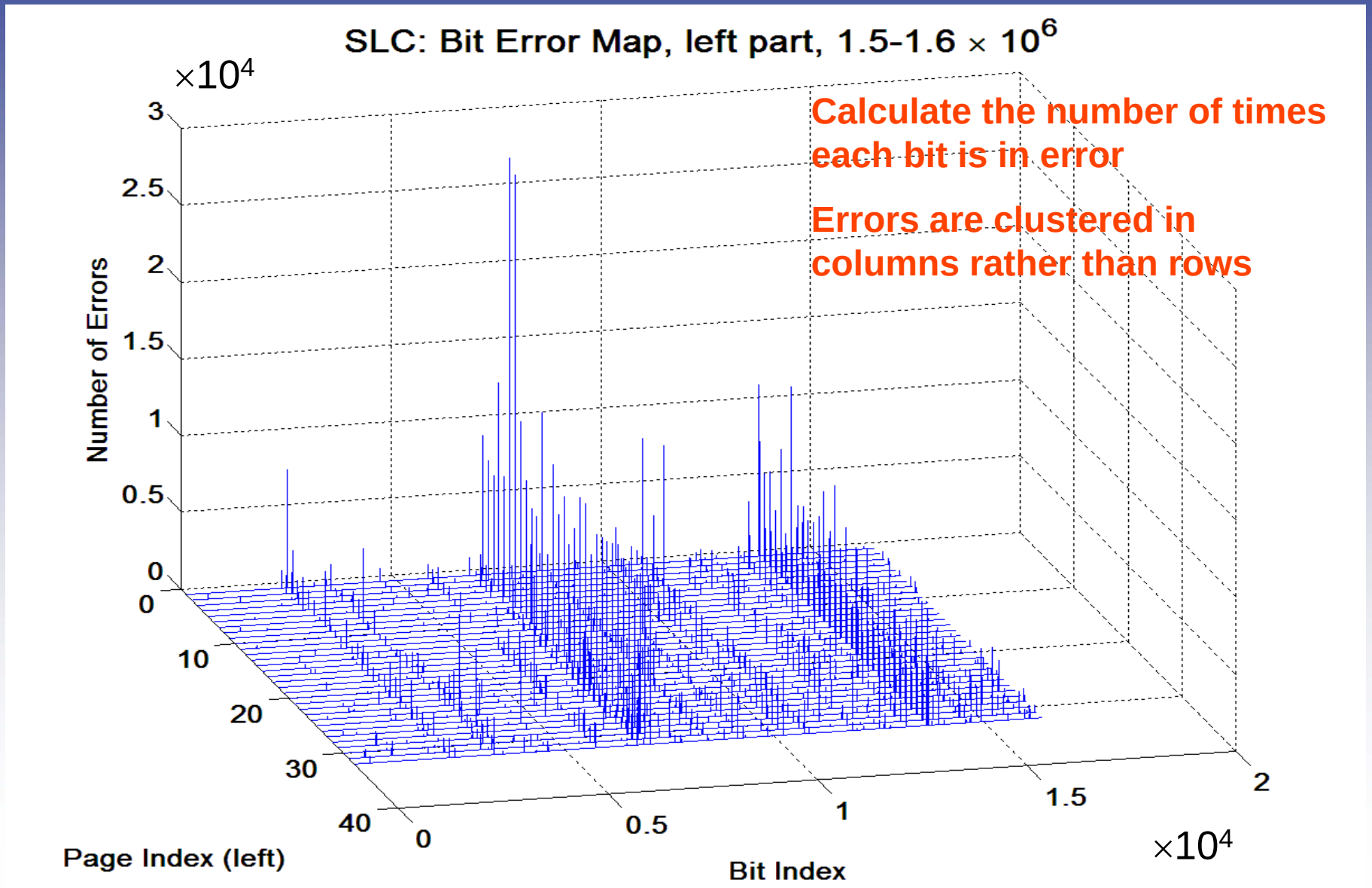
MLC - BER Page Dependency



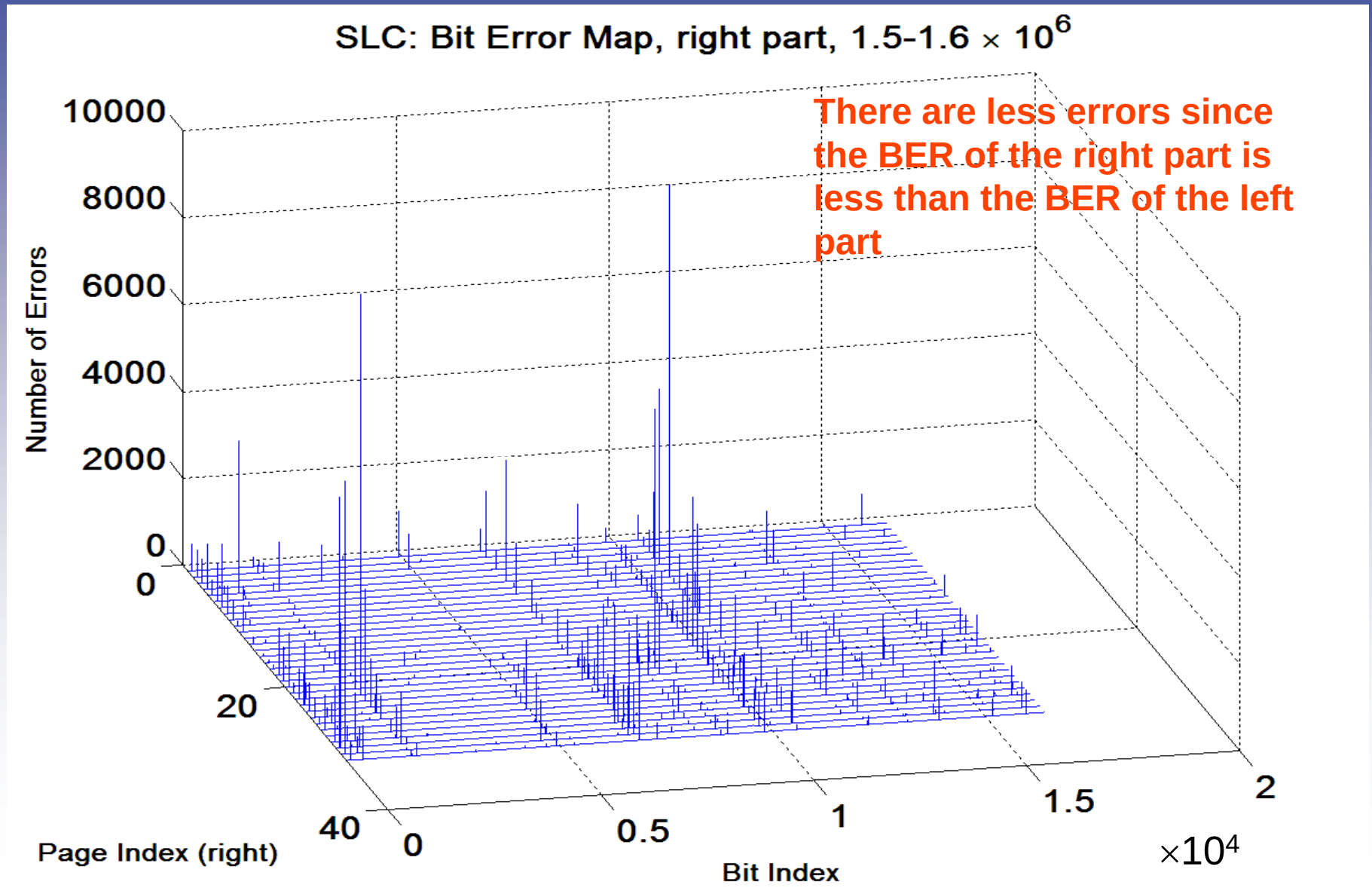
SLC - Bit Error Map

- We checked how the errors behave for each bit
- For a small window of iterations, **$1.5\text{-}1.6\times10^{6}$** iterations - the BER is roughly fixed, we checked for each bit the number of times it was in error

SLC - Bit Error Map for Odd Pages



SLC - Bit Error Map for Even Pages



ECC Comparison

- We compare between **BCH**, **RS** and **burst-correcting codes**
- We compute the **BER** and **PER** assuming we used for each of these codes the same number of redundancy bits
- Best results are achieved for **BCH codes**
- We have another scheme for correcting in the entire block in two levels:
  - **First level**: correct and detect errors in each page
  - **Second level**: if there are errors that were detected and not corrected in the pages, use the last redundancy page(s) to correct them
- We could improve the lifetime by **~14%**

  Lifetime - first errors occurrence

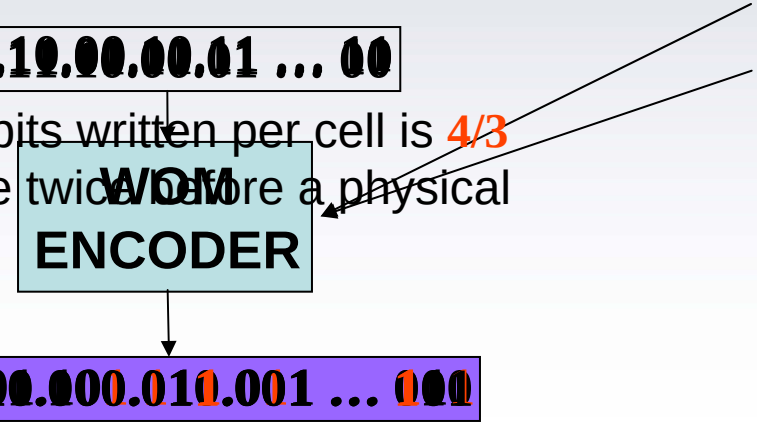
Write Once Memory (WOM) Codes for SLC

- A scheme for storing two bits twice using only three cells **before erasing the cells**
- The cells only **increase** their level
- How to implement? (in **SLC** block)
  - Each page stores **2KB/1.5 = 4/3KB** per write
  - A page can be written twice before erasing
  - Pages are **encoded** using the **WOM code**
  - When the block has to be rewritten, mark its pages as **invalid**
  - Again write pages using the WOM code **without erasing**
  - **Read before write** at the second write

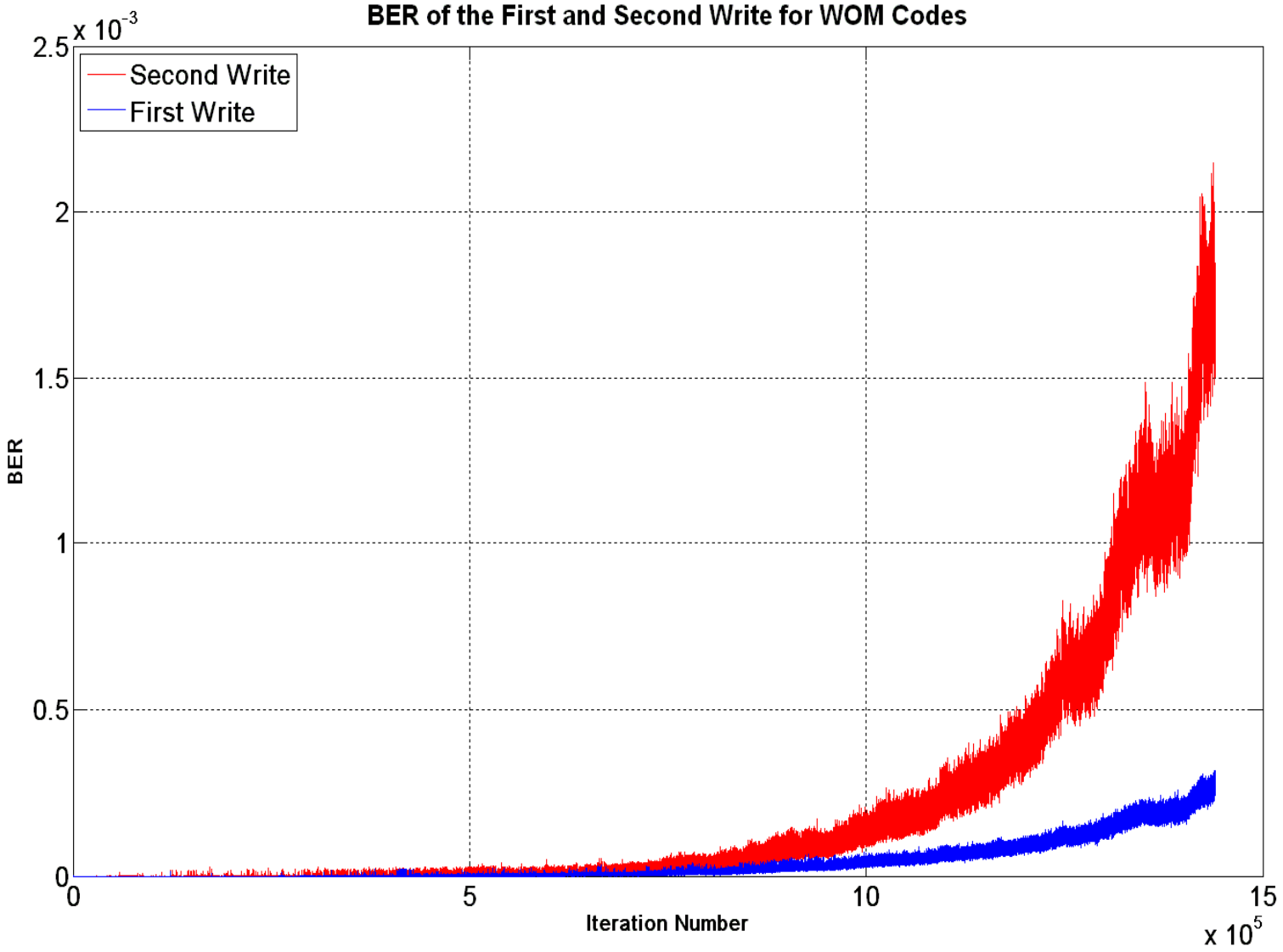
data	1st write	2nd write
00	000	111
01	100	011
10	010	101
11	001	110

Cells state

Advantages:
- The number of bits written per cell is **4/3**
- Possible to write twice before a physical erasure



BER for the First and Second Writes



Summary

- Error characterization in flash memories
- Comparison between potential codes
- ECC for the entire block
- Write Once Memory (WOM) codes
- More analysis of codes and error behavior -

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