Improving System Performance and Longevity with a New NAND Flash Architecture

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Agenda

- Background
- Technical Innovations
- Solutions for Emerging Applications
- Summary
NAND Technology Timeline

- **1984**: NAND Cell Invented
- **1987**: 2Mb NAND Prototype & 1st Specification
- **1992**: Entered Gb Flash Era (1Gb NAND Flash Developed in 90nm)
- **1995**: SSD Emerged (8Gb SLC & 16Gb MLC in 50nm)
- **2002**: MCL (2bits/cell) for Mainstream (4Gb SLC & 8Gb MLC in 65nm)
- **2005**: 3bits/cell & 4bits/cell (32Gb MLC in 34nm)
- **2007**: Confirmed NAND Technology & Manufacturability
- **2009**: Key Circuit Techniques (Self-boosting, ISSP) Reported (32Mb NAND Developed)

**Reported (32Mb NAND Developed)**
The single-minded focus on bit density improvements has brought Flash technology to current multi-Gb NAND devices.
**NAND Architecture Trend**

- Primary focus is density for cost and market adoption
- Page-based program and block-based erase

**Diagram**

- **A:** # of Bit/Cell
  - 1
  - 2
  - 3
  - 4

- **B:** # of Bitline/Page Buffer
  - 1
  - 2
  - 4

- **C:** # of Cell/NAND String
  - 8
  - 16
  - 32
  - 64

- **D:** Page Size
  - 512B
  - 2KB
  - 4KB
  - 8KB
  - 16KB

**Block Size** = \((A \times B \times C) \times D\)

Erase Program Mismatch (EPM) = \(A \times B \times C\)
Erase Program Mismatch (EPM) is a key parameter to degrading write efficiency (i.e. increase write amplification factor)
Reliability degradation combined with the current NAND architecture trend introduces a negative impact on computing applications.
System lifetime heavily relies on NAND architecture and features

\[
Write \ Efficiency = \frac{\text{Total Data Written by Host}}{\text{Total Data Written to NAND}}
\]

\[
\text{Total Host Writes} = \text{NAND Endurance Cycle} \times \begin{cases} \text{System Capacity} \\ \text{Write Efficiency} \\ \text{Wear Leveling Efficiency} \end{cases}
\]

\[
\text{System Lifetime} = \frac{\text{Total Host Writes}}{\text{Host Writes per Day}}
\]
Block Size = (A * B * C) * D
NAND Architecture Innovation

FlexPlane with 2-tier Row Decoder Scheme

- Smaller & Flexible Page Size (2KB/4KB/6KB/8KB)
- Smaller & Flexible Erase Size
- Lower power consumption due to segmented pp-well
- Extend system lifetime

### FlexPlane Operations

- NAND Cell Array on Sub PP-Well
- Segment Row Decoder
- NAND Cell Array on Sub PP-Well
- Segment Row Decoder
- NAND Cell Array on Sub PP-Well
- Segment Row Decoder
- NAND Cell Array on Sub PP-Well
- Segment Row Decoder
- Global Row Decoder

- 2KB Page Buffer
- 2KB Page Buffer
- 2KB Page Buffer
- 2KB Page Buffer
NAND Architecture Innovation

2-Dimensional Page Buffer Scheme

- Higher Performance
- Lower Power Consumption
- Higher Yield

2-Dimensional Page Buffer
(Shared Page Buffer)

0.5x Bitline Length compared to conventional NAND architecture

Micron 32Gb NAND Flash in 34nm, 2009 ISSCC
- Minimize Erase Program Mismatch (EPM)
- Improve write efficiency

• MOSAID’s Erase Scheme*

> Minimize Erase Program Mismatch (EPM)
> Improve write efficiency

NAND Core Innovation
Lower Operating Voltage

2.7 ~ 3.6V
H.V. Gen
Core and Peri.
I/O

2.7 ~ 3.6V
H.V. Gen
Core and Peri.
I/O

3.3V
1.8V
H.V. Gen
Core and Peri.
I/O

• MOSAID’s Low Stress Program Scheme*

HyperLink (HLNAND™) Flash

MCP HLNAND

Monolithic HLNAND

- Fully independent bank operations
- Multiple, simultaneous data transactions
- Data throughput independent of core operations
- Device architecture for performance and longevity
  - FlexPlane Architecture
  - Two-dimensional Page Buffer
  - Two-tier Row Decoder

- NAND flash cell technology
- Page/multipage erase function
- Partial block erase function
- Low stress program scheme
- Random page program in SLC
- Low Vcc operations

- Device interface
  - independent of memory technology and density
- Packet protocol with low pin count
- Configurable data width link architecture
- Flexible modular command structure
- Simultaneous Read and Write
- EDC for command and ECC for registers
- Daisy-chain cascade with point-to-point connection of up to virtually Unlimited number of devices
HyperLink Interface

- **Point-to-point ring topology**
  - Synchronous DDR signaling with source termination only
  - Up to 255 devices in a ring without speed degradation
  - Dynamically configurable bus width from 1-8 bits
  - HL1 parallel clock distribution to 266MB/s
  - HL2 source synchronous clocking to 800MB/s, backward compatible to HL1

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Host Interface

Controller

HLNAND

HLNAND

HLNAND

HLNAND
64Gb MLC HLNAND MCP

- HLNAND bridge chip MCP with 4-NANDs stacked
- HL1 (DDR-200/266) using NAND in MCP - fully compliant to HLNAND spec

12 x 18 100-Ball BGA
HLNAND Flash Module (HLDIMM)

- Use cost effective DDR2 SDRAM 200-pin SO-DIMM form factor and sockets
- 8 x 64Gb or 8 x 128Gb HLNAND MCP (4 on each side)
HLDIMM Port Configuration

- Four independent HyperLink interface (266MB/s)
- Aggregate bandwidth of 1066MB/s regardless of # of module
HLDIMM Pin Assignment

- All high speed signals fully shielded with 1:1 ratio between signal and power/ground
- 6 Vss, 3 Vdd (1.8V), 3 Vdd3 (3.3V) per channel in/out
- Vref and Reset pins shared by all channels
- 5 pin SPD interface
- Forward compatible to HL2 800MB/s source synchronous clocking
System Configurations with HLDIMM

Non-Interleave - 1066MB/s Aggregate Throughput

Interleave - 2133MB/s Aggregate Throughput
HLDIMM Performance
Capacity, Bandwidth and Random IOPS

Capacity & Bandwidth vs. # of Modules

Random IOPS vs. # of Modules
Fully populated memory capacity of 512GB or 1TB is achieved using 64GB and 128GB HLDIMM modules within only 60cm² of motherboard area.
The driving forces in future Flash memory are the memory architecture & feature innovation that will support emerging system architectures and applications.

Using HLNAND Flash, Storage Class Memory is viable today using proven NAND flash technology.
Available
- 64Gb MLC MCP sample
- 64GB HLDIMM sample
- Architectural Specification
- Datasheets
- White papers
- Technical papers
- Verilog Behavioral model