Toggle-Mode NAND to Fill Growing Need for Higher Performance

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Process Technology Evolution

Density Keeps Increasing

Performance & Reliability Concerns !!!

90nm 70nm 60nm 50nm 40nm 30nm 20nm
Growing Need for Higher Performance - Interface Speed Trend

- SATA 3
- SATA 2
- SATA 1
- UFS
- MMC 4.4
- MMC 4.3
- USB 3.0
- USB 2.0
- SD 3.0 UHS-2
- SD 3.0 UHS-1
- SD 2.0

I/F Speed (Per Pin) vs BW

Santa Clara, CA  USA
August 2009
Growing Need for Higher Performance
- NAND Performance Requirement

- PCIe3.0 (x16, 32ch)
- 250 Mbps
- PCIe2.0 (x4, 10ch)
- 200 Mbps
- USB3.0 (x1, 4ch)
- 150 Mbps
- PCIe2.0 (x1, 4ch or x4, 16ch)
- 100 Mbps
- SAS6G (x1, 16ch)
- 50 Mbps
- SD3.0 (UHS2, x4, 2ch)
- 40 Mbps, Legacy NAND

Santa Clara, CA USA
August 2009

* Only I/F BW translated. If considering latency, min requirement would be increased
Market Expansion

- Enterprise-class SSD (SATA3, SAS, PCIe) and high-speed card (USB3.0, UHS2, UFS) are fueling the need of higher performance NAND.

- Enterprise SSD will take ~65% of SSD market at 2012.

- USB will take ~14% of NAND market at 2012.

- SD & uSD will take ~80% of flash card market at 2012.
High speed “Toggle-Mode” operation

- No clock – Asynchronous Double Data Rate
- High performance by using the asynchronous interface for backward compatibility
- Bidirectional DQS for read and write operations
Why Toggle-Mode NAND?

- High performance
  - Supports 133Mbps and higher

- Less power consumption
  - No free-running clock

- Flexibility of operating frequency
  - No additional mode change required

- Easy migration from legacy NAND
  - Same signal functionality as legacy NAND
Differentiation from Others

- No free-running clock
  - Less power consumption
  - Free from IP issues

- Flexibility of operating frequency
  - No additional mode-set change required

- Simple adoption
  - Same signal functionality as legacy NAND
Development Status & Roadmap

- 1\textsuperscript{st} Gen available 2H ’09 at 133Mbps
- 2\textsuperscript{nd} Gen(200Mbps) targeted for early’11, but entry time depends on market needs and requirements

<table>
<thead>
<tr>
<th></th>
<th>’09</th>
<th>’11 or earlier?</th>
<th>~’13(Investigating)</th>
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</thead>
<tbody>
<tr>
<td>Gen 1</td>
<td>133Mbps</td>
<td></td>
<td></td>
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<tr>
<td>Gen 2</td>
<td>200Mbps</td>
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<tr>
<td>Gen 3</td>
<td>400Mbps</td>
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## Standardization Status in JEDEC

<table>
<thead>
<tr>
<th>Item</th>
<th>Status</th>
<th>Comments</th>
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<tbody>
<tr>
<td>Packaging &amp; Pin-out</td>
<td>On Going</td>
<td>Ball Configuration Done</td>
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<tr>
<td>Addressing &amp; Bad Block Definition</td>
<td>Done</td>
<td></td>
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<tr>
<td>Signal Definition</td>
<td>On Going</td>
<td>Under Documentation</td>
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<tr>
<td>AC Parameter</td>
<td>Done</td>
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<tr>
<td>Initialization &amp; Identification</td>
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<tr>
<td>Timing/Command Set</td>
<td>On Going</td>
<td>Basic Command Set Done</td>
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<td>Interface &amp; I/O Characteristics</td>
<td>On Going</td>
<td>AC/DC &amp; Operating Condition Done</td>
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<tr>
<td>Parameter Page Definition</td>
<td>On Going</td>
<td>Byte[100:0] Done</td>
</tr>
</tbody>
</table>
Thank You!

For more information,
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