



Flash Firmware Secrets Revealed

Jim Fitzpatrick

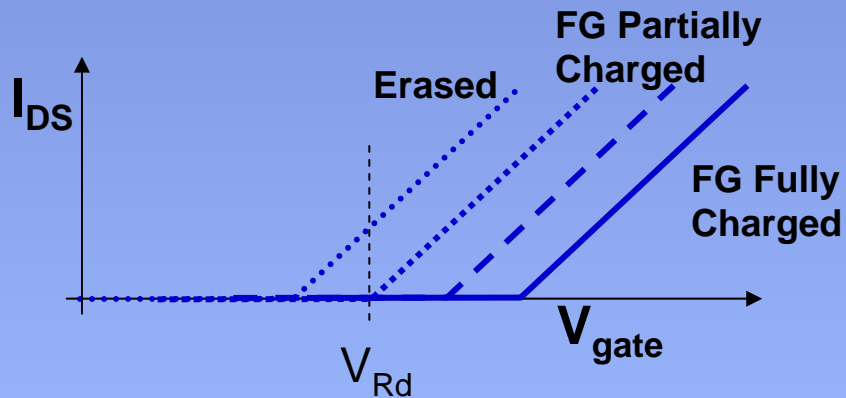
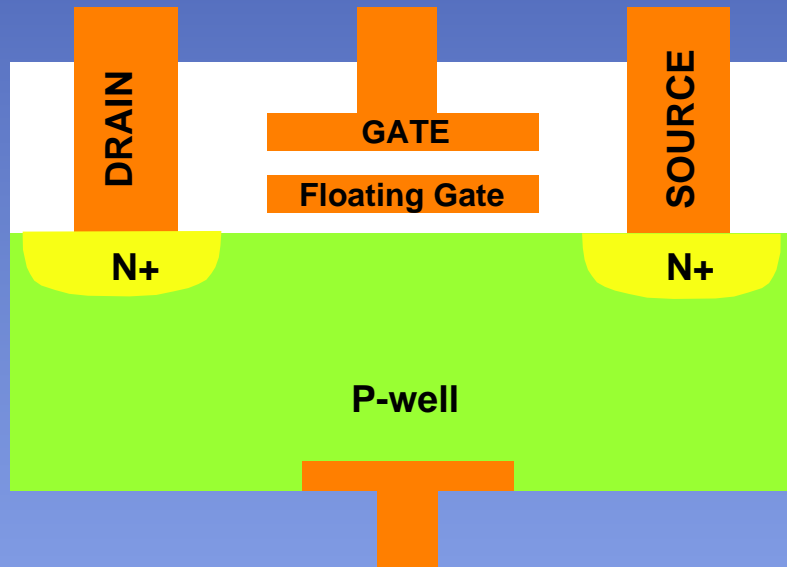
Smart Modular Technologies

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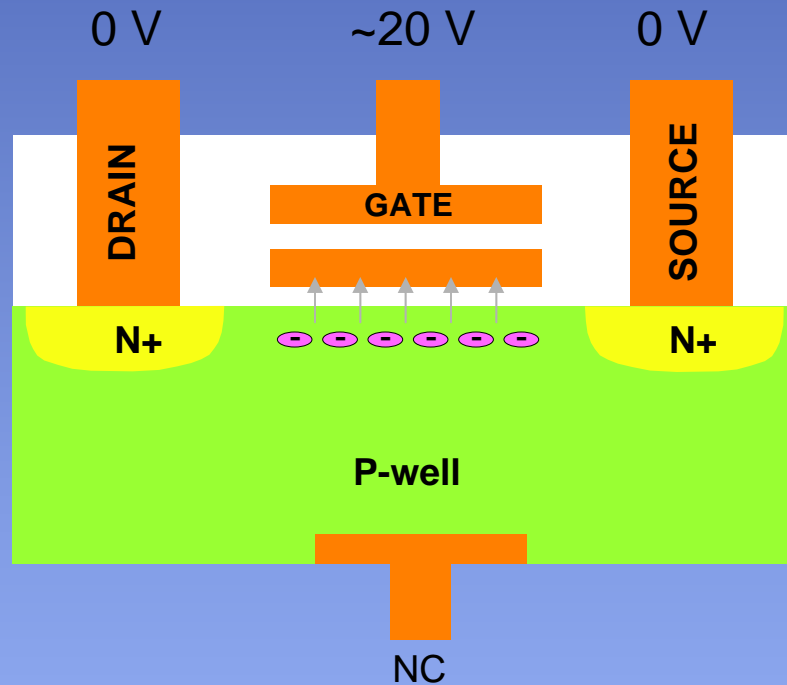
- Objective is to use NAND flash beyond its guaranteed life by exploiting knowledge of failure mechanisms.
- Program Erase Cycling and Read Disturbs can cause excessive error rate.
 - Goal: model error rate degradation as a function of both PE cycles & read disturbs so that firmware can optimally wear level.
 - With accurate modeling of block life, it is possible to improve the choice of block to recycle.
- The focus of this presentation is on improving models of PE & read disturb effects through measured data.

Floating Gate NAND Cell

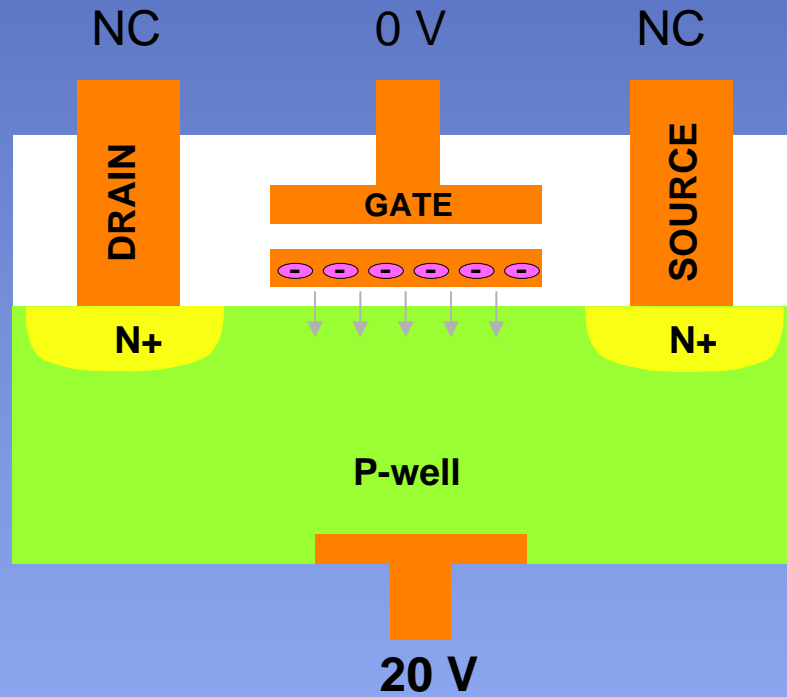


- Charge on floating gate is trapped by the surrounding insulator.
- V_{TH} shifts to a higher voltage in proportion to the amount of charge trapped on the floating gate.

Programming

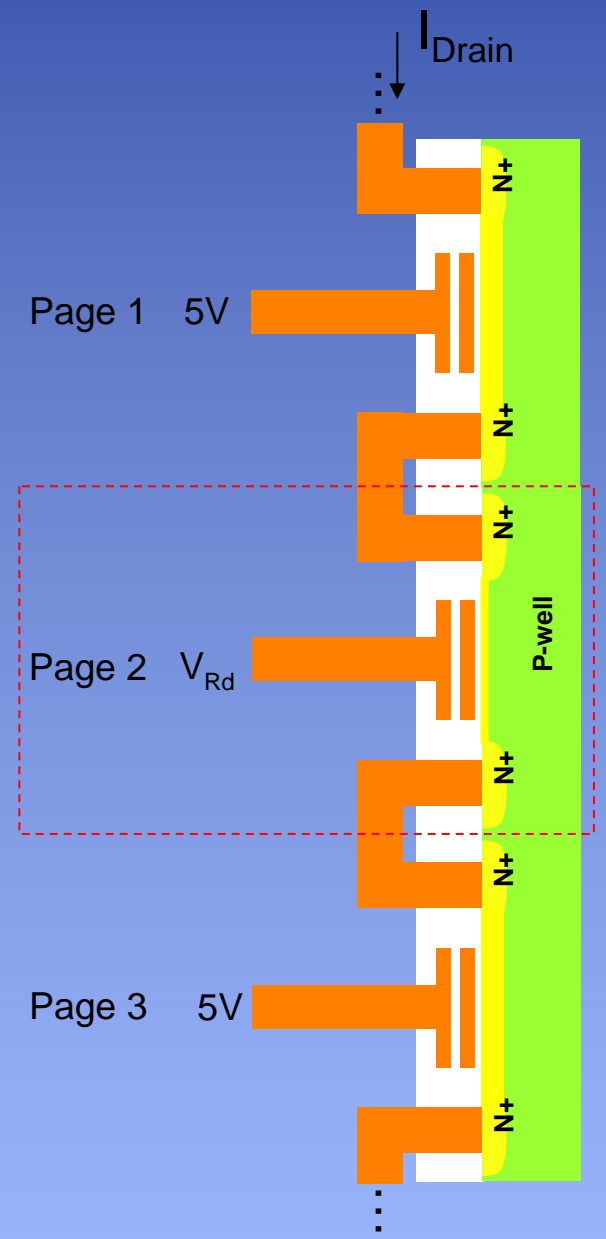
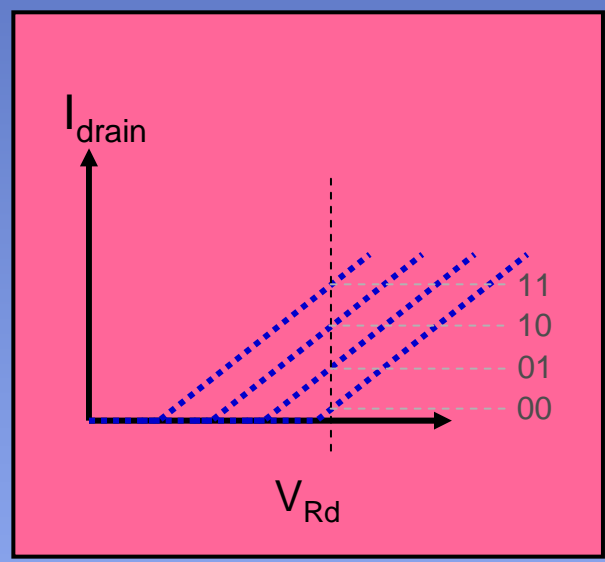
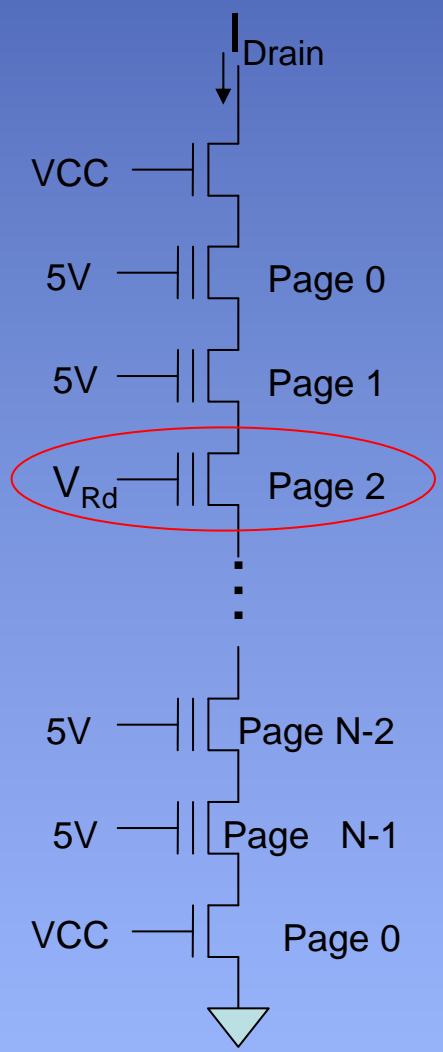


Erasing

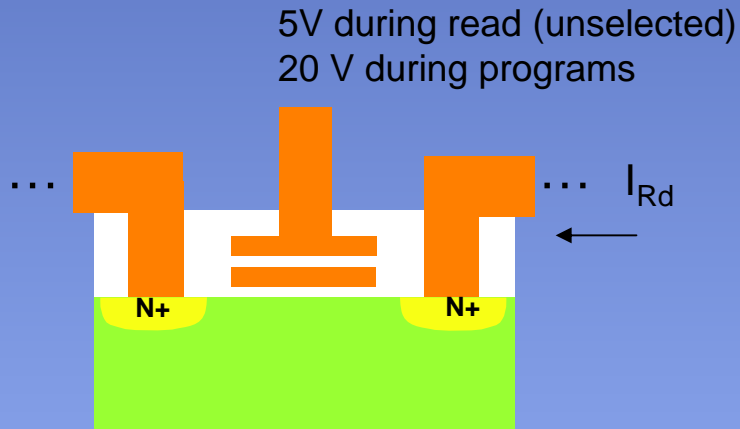




Flash Memory Reading



Read Disturbs



- Unselected cells receive a voltage that mimics a low voltage program.
- The relative size of the energy barrier that keeps electrons from populating the floating gate is lowered during reads.
- Program / Erase cycles damage the insulator, thus lowering the energy needed to transfer electrons to the FG.



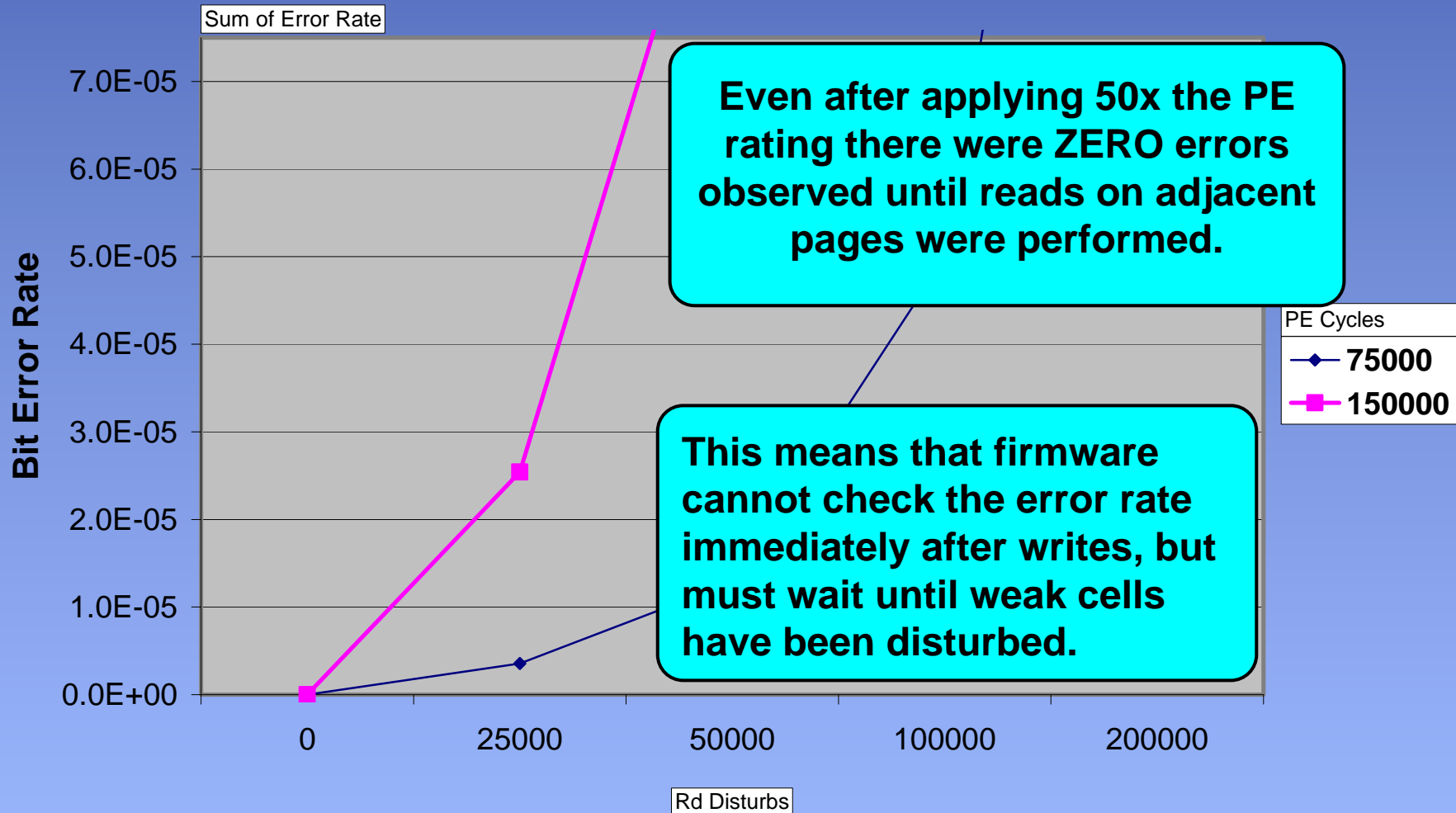
Flash Memory Experiment

- PE Loop
 - Apply N Program / Erase cycles (50% 1's, 50% 0's)
 - Rd Disturb Loop
 - Write all pages once
 - Apply K Reads to pages 2-5
 - Read all pages except 2-5 once, then report error rate
 - End Rd Dist Loop
- End PE Loop

- Results reported here are at room temperature.
- Data shown here is from a single chip
- PE rating is nominally 3000 cycles for this design.

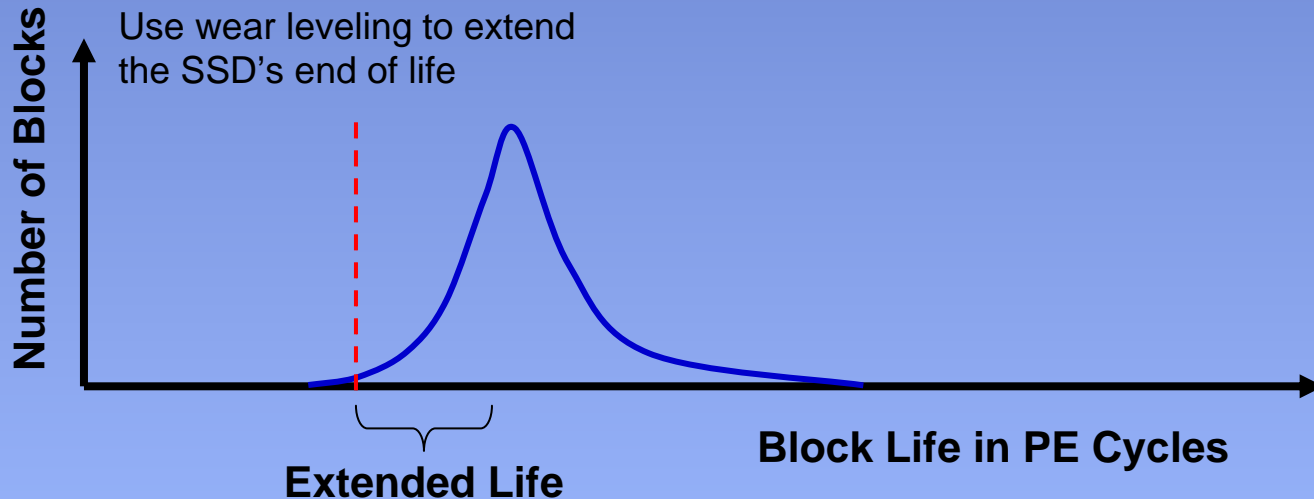
BER without Read Disturbs

BER vs Number of Read Disturbs



Block Lifetime and Wear Leveling

- If some blocks have substantially more life than others, the healthy blocks can be used more frequently to extend the life of the flash beyond the minimum.

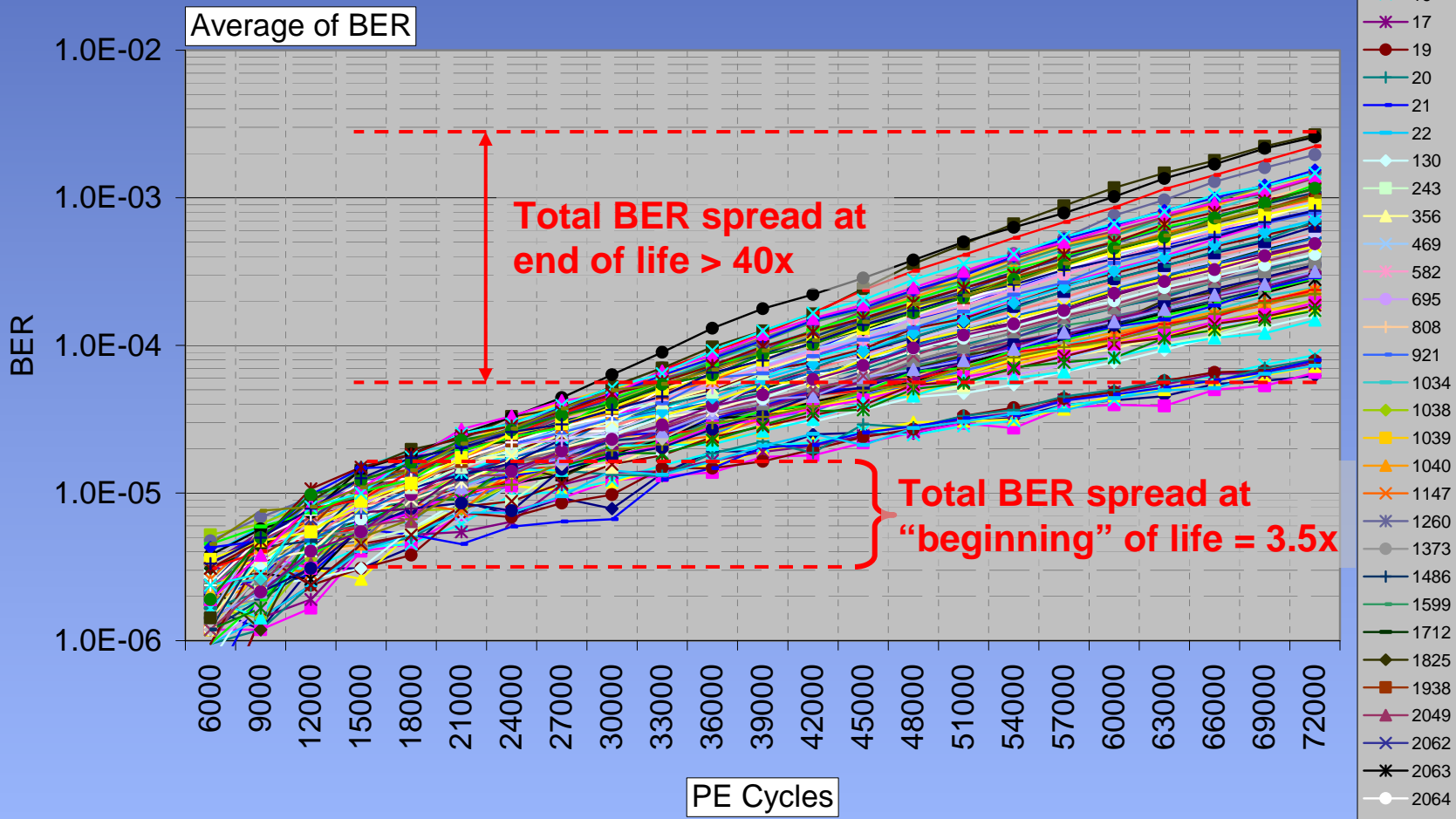




Block BER vs Number of PE Cycles

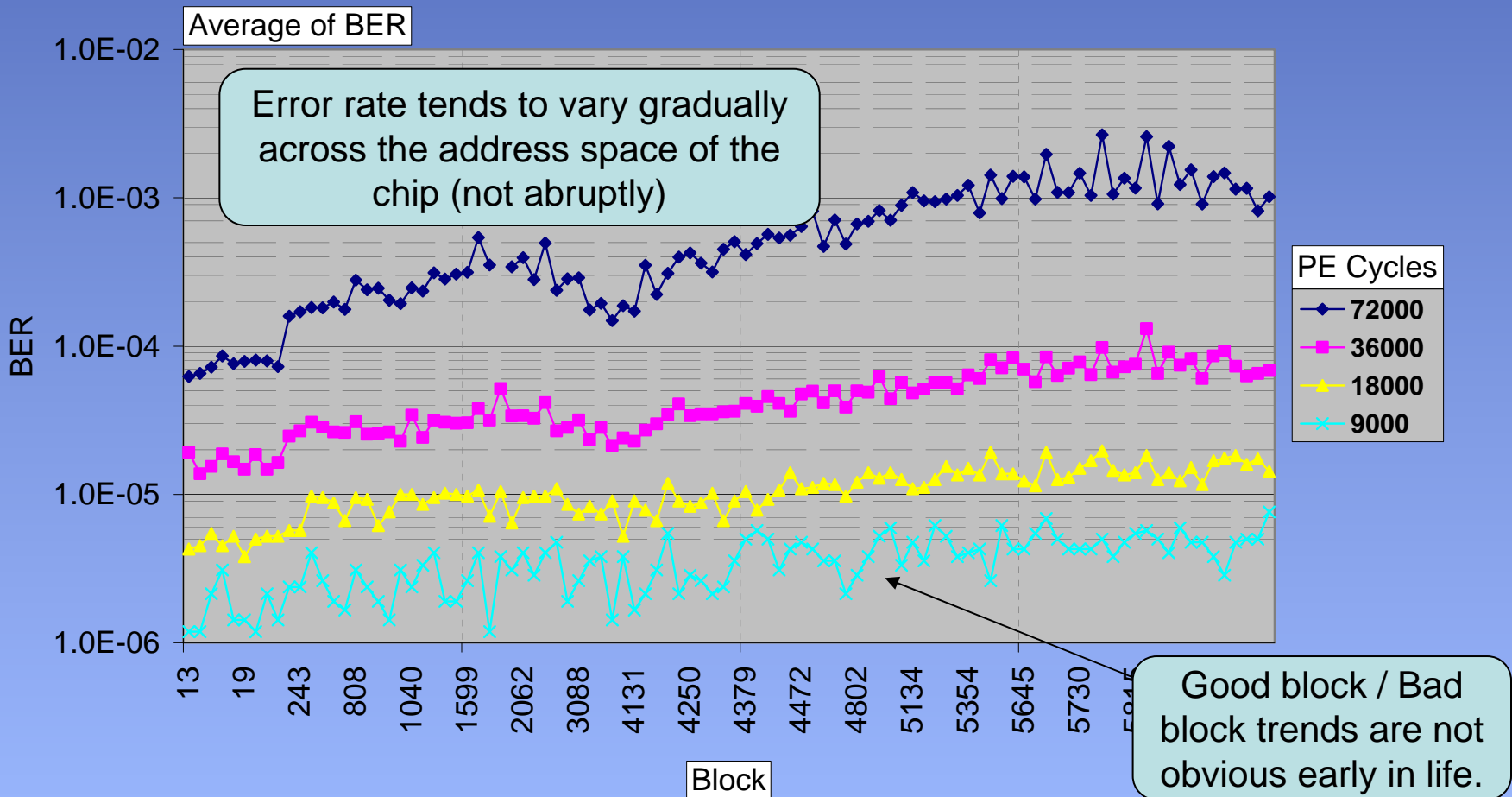
Rd Disturbs 100000

Avg BER vs Number of and PE Cycles and Read Disturbs

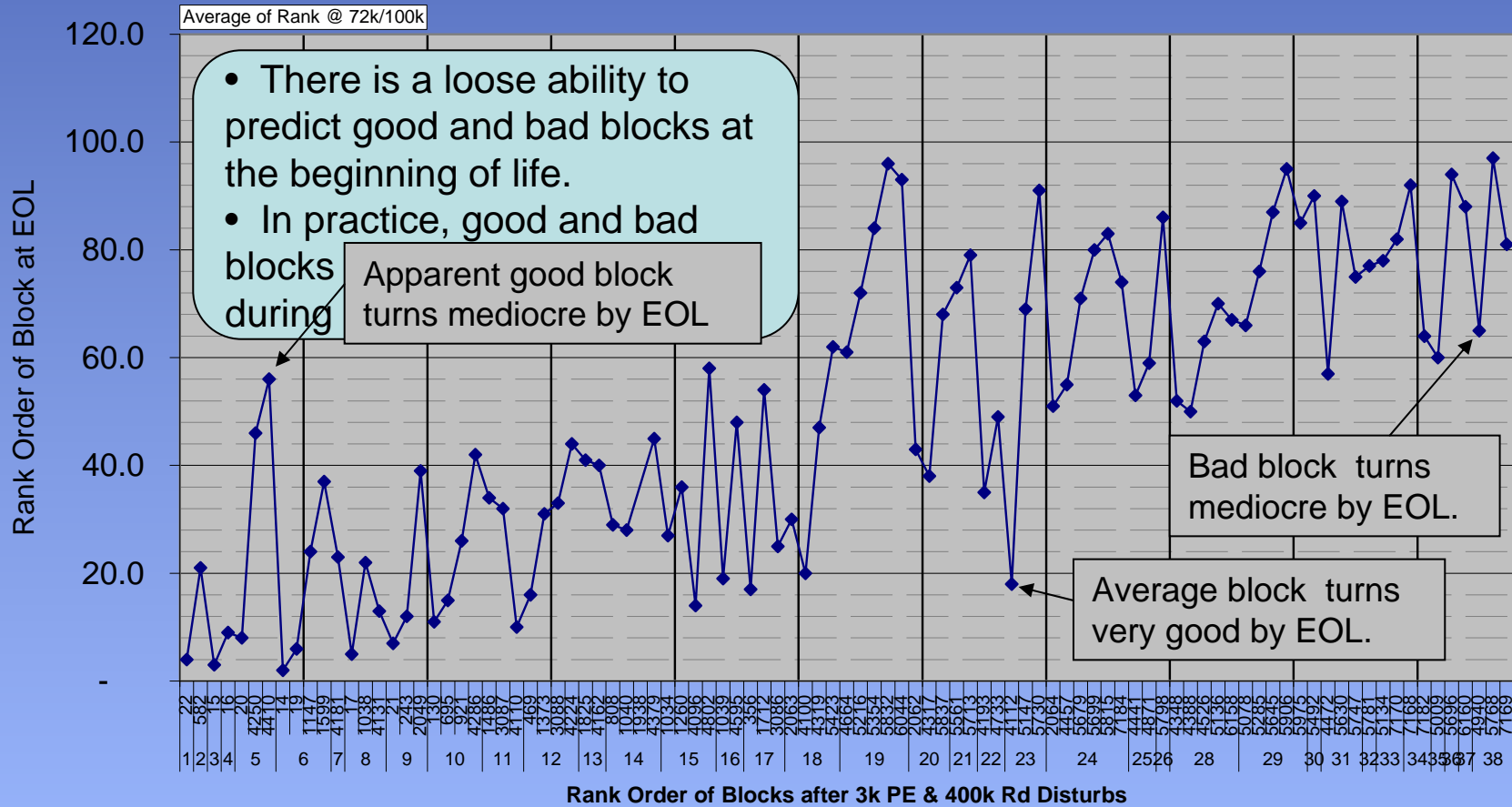


Rd Disturbs 100000

BER vs Block Number and Number of PE Cycles

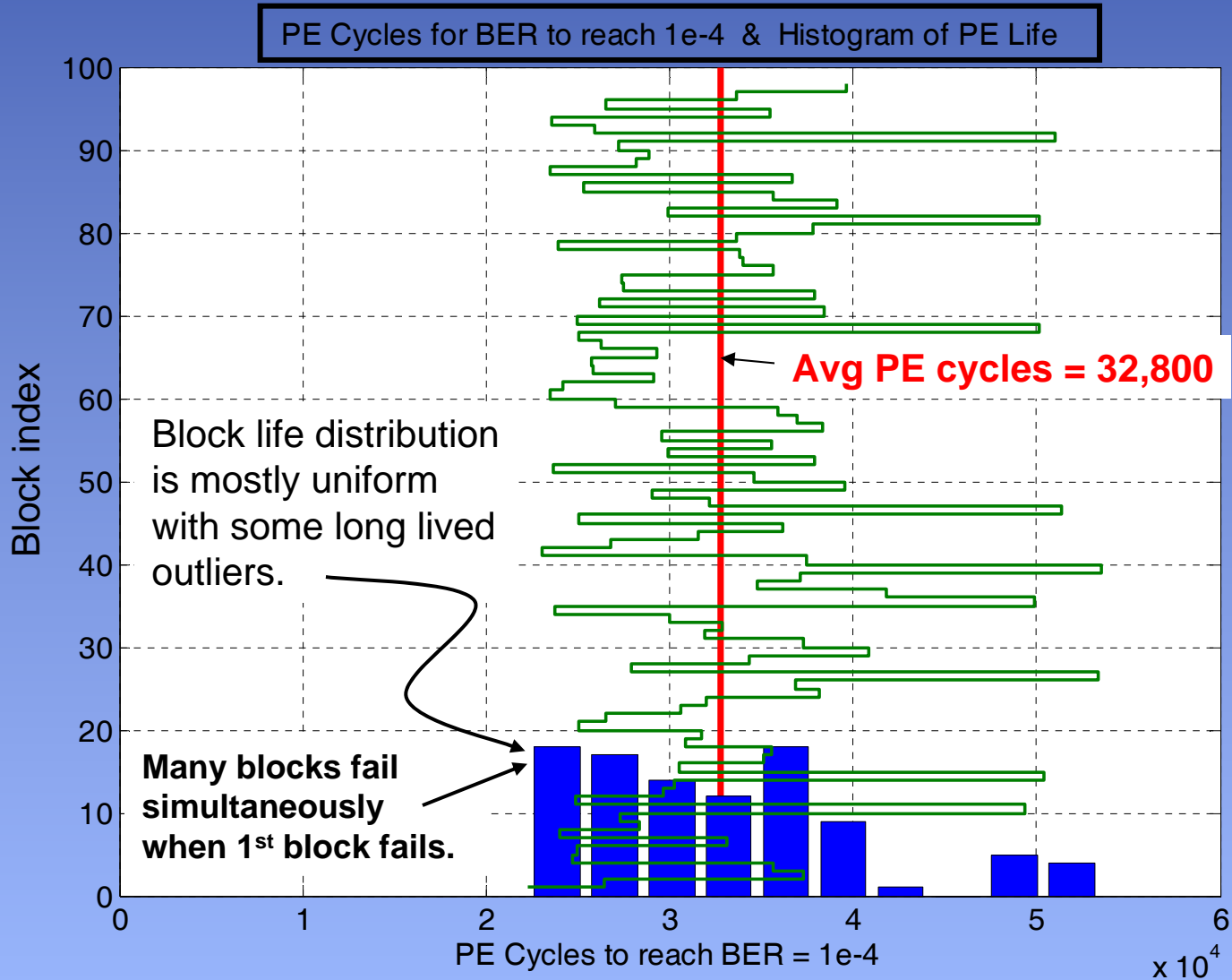


Rank Ordering at EOL vs Rank Ordering at Beginning of Life



Rank @ 3k / 400k | Block

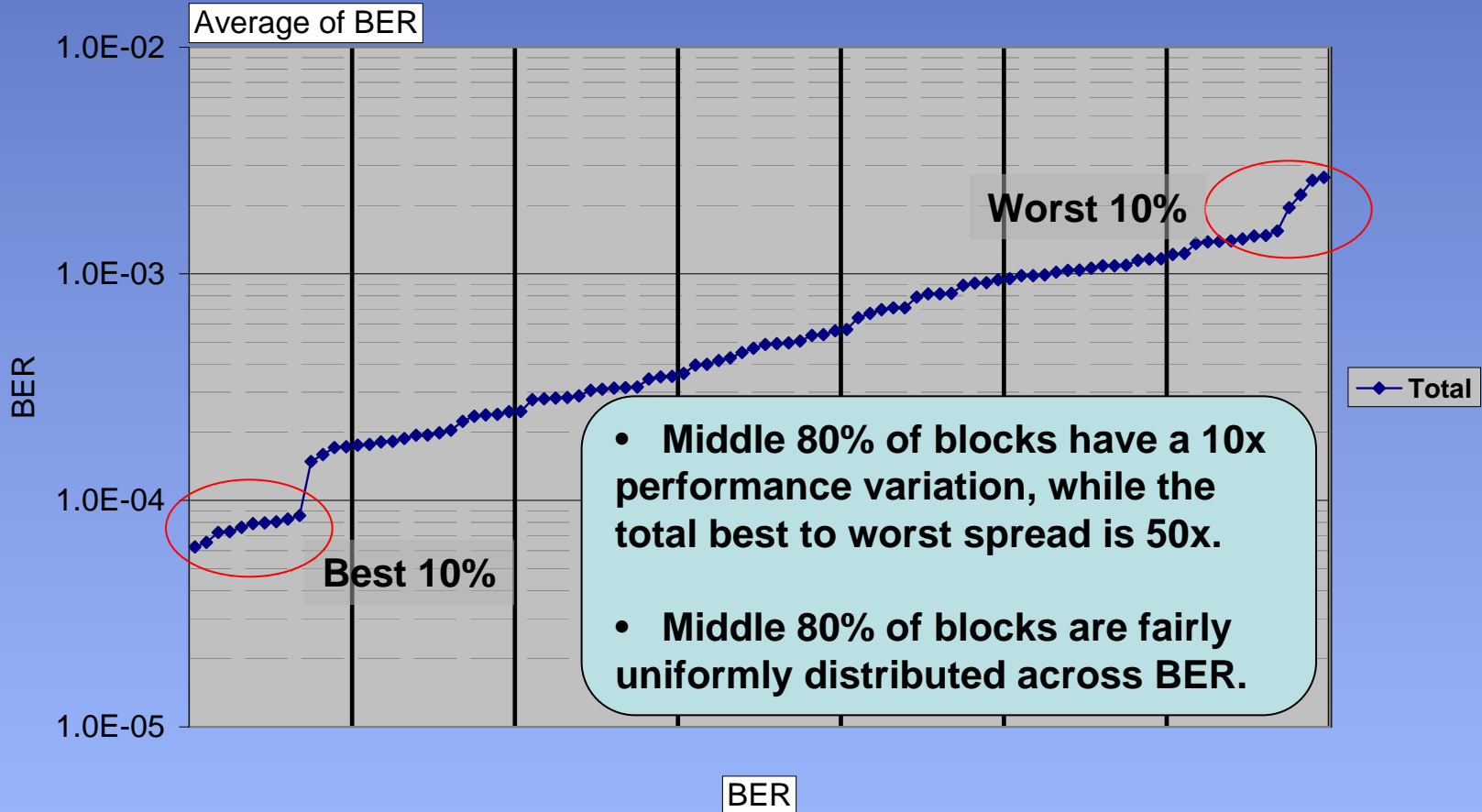
Distribution of Block Life (after 200k Reads)



Sorted BER for 72k PE / 100k Rds

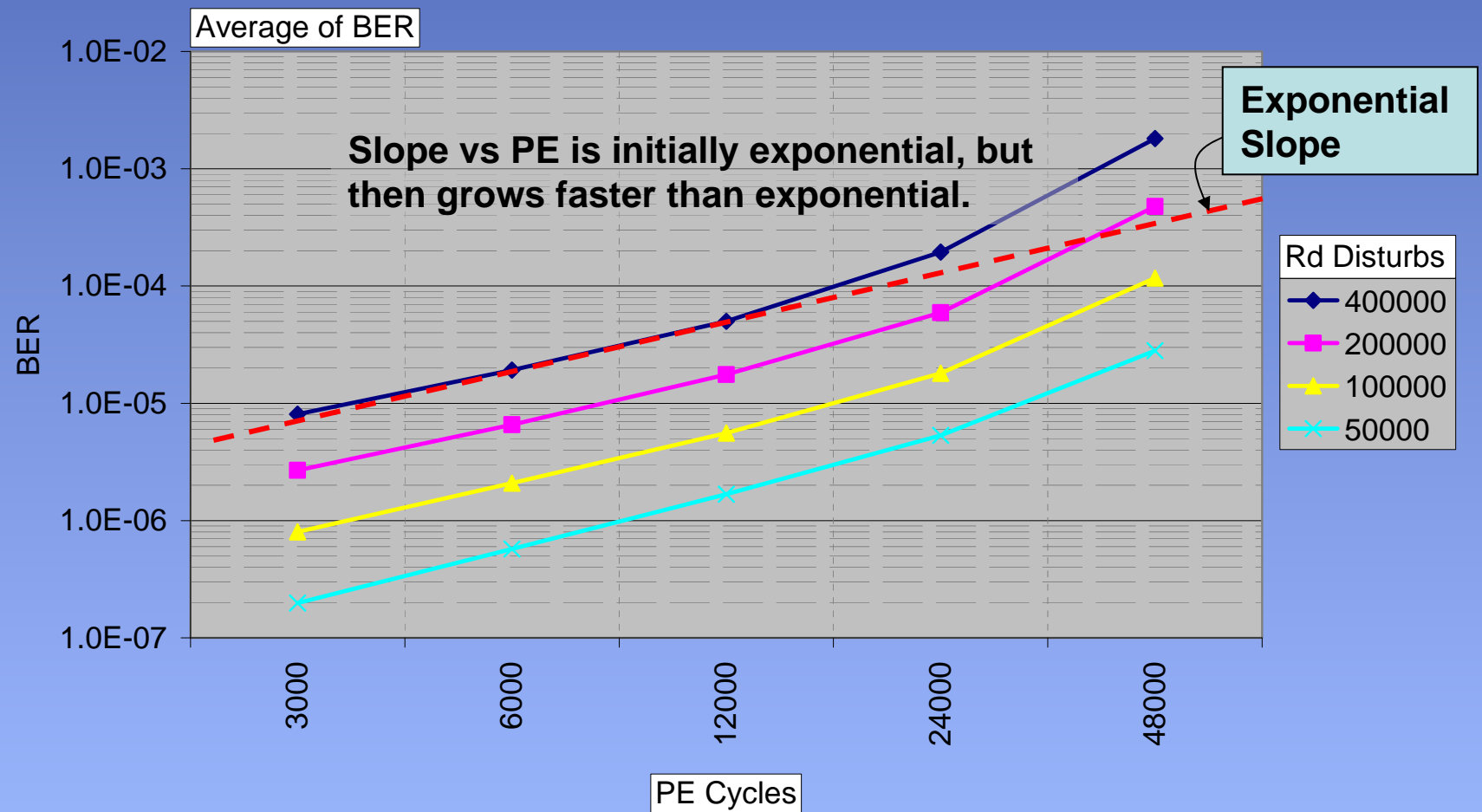
PE Cycles 72000 | Rd Disturbs 100000

BER sorted from Best to Worst



BER vs PE & Read Disturbs

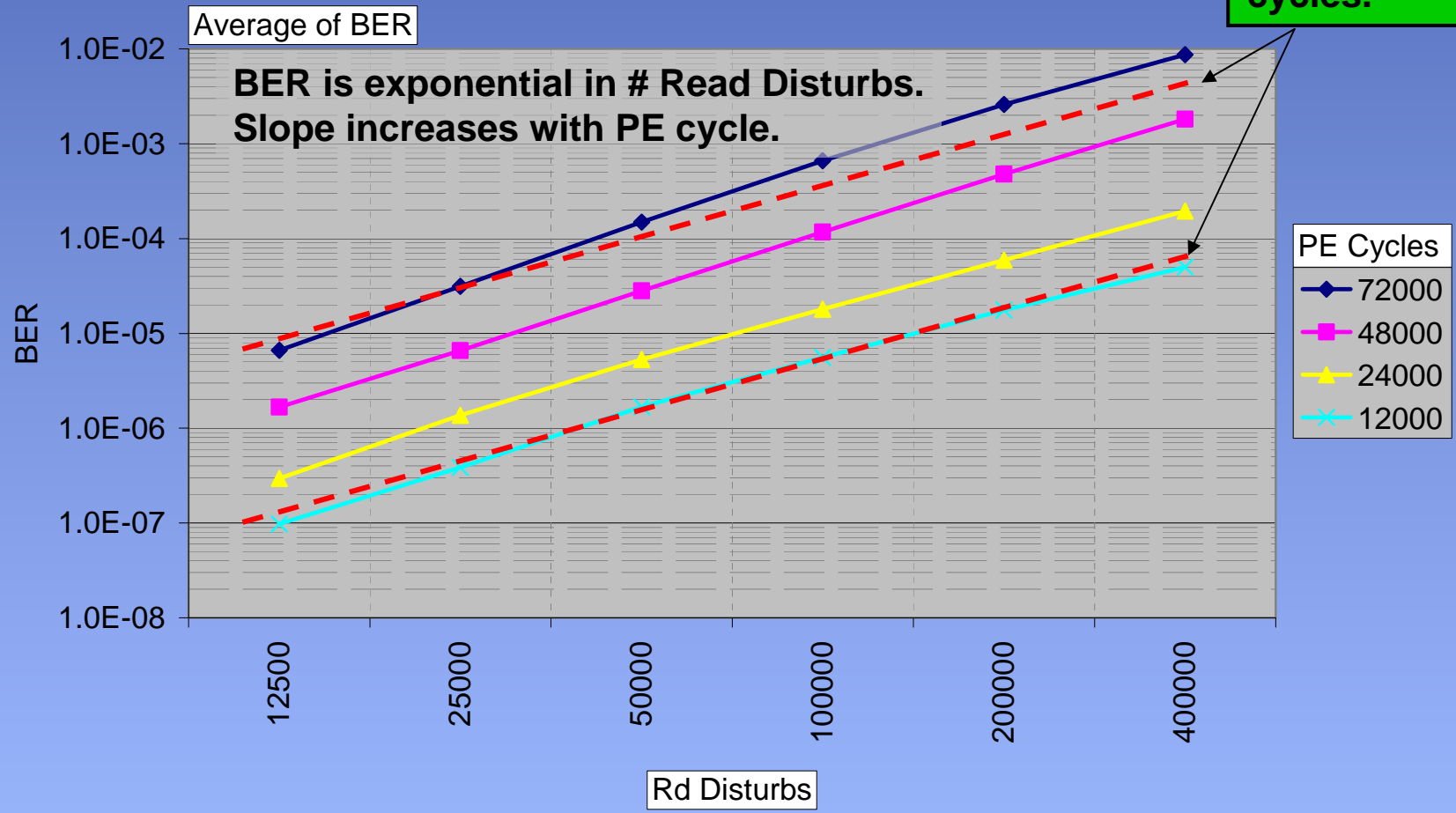
Avg BER vs PE Cycle & Number of Read Disturbs



BER vs Read Disturbs & PE Cycles

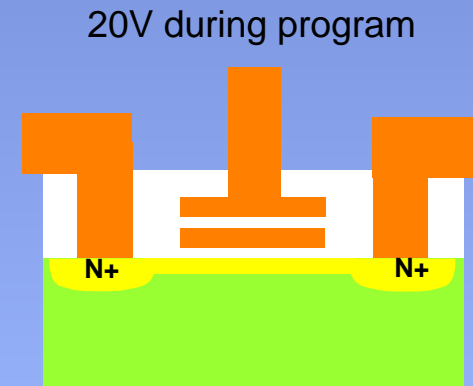
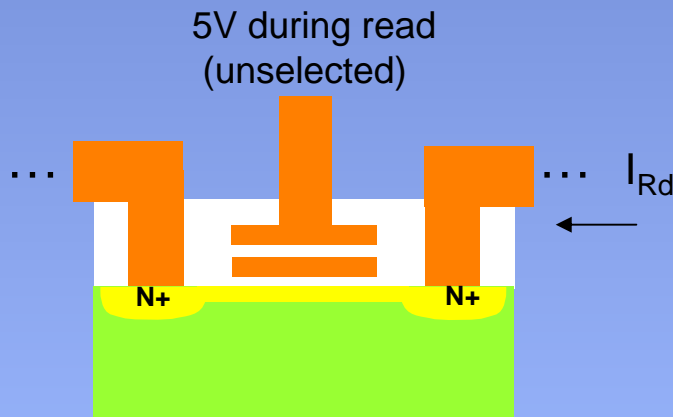
Avg BER vs Number of Read Disturbs and PE Cycles

Increased slope after many PE cycles.



Arrhenius Modeling

- Read disturbs behave as if each read of an adjacent page provides an opportunity for electrons to exceed the energy barrier needed to get to the floating gate.
- Increasing PE cycles causes the “activation energy” to increase and accelerate the effects of read disturbs.



- Simple Model for Wear
 - BER is exponential vs the number of read disturbs
 - BER grows faster than exponential vs the number of PE cycles.
- Block Life
 - Predicting block life from early life measurements captures trends, but misses many exceptional blocks.
 - Block performance is generally well correlated with adjacent block performance.