Forum F1B/F2B: Flash Memory-Based Architectures: A Technical Discussion

Brian A. Berg / Berg Software Design
bswd.com
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- Kay Firmware Architectural Issues:
  - Data integrity, availability and reliability
  - How performance affects cost and architecture
  - Flash Translation Layer (FTL)
  - Standards efforts regarding flash allocation defragmentation issues (e.g., the TRIM command)
  - Interface (e.g., SATA/SAS/USB v. PCIe)
  - How and where ECC is performed
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• You will hear discussions related to these topics throughout the conference
• These topics must be addressed in some fashion by any flash-based device
• Today’s Goal: 
  
  *Gain an understanding of these topics*
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• Four morning talks (F1B):
  1. Michael Abraham, Micron: architectural overview
  2. Gary Orenstein, Fusion-io: Flash Translation Layer
  3. Jeremy Werner, SandForce: MLC in the enterprise; end-to-end data protection
  4. Holly Frost, Texas Memory Systems: SLC in the enterprise; controller “secret sauce”
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- Four afternoon talks (F2B):
  1. Eyal Bek/Avi Klein, SanDisk: multitasking firmware
  2. Swapna Yasaranpu, STEC: MLC in the enterprise; benchmarking SSDs
     Up a notch in the “storage stack”:
  3. Sudipta Sengupta, Microsoft Research: application software layer: flash performance innovation
     Up another notch in the “storage stack”:
  4. Andy Walls, IBM Almaden Research Center: Data Center architecture based on SSD architecture
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- All conference presentations will eventually be on the FMS website
- All F1B/F2B presentations are currently on my website at www.FlashCornucopia.com
- This site also includes presentations from my FMS sessions going back to 2007, and much more
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• About myself:
  • Independent consultant
  • Software and firmware developer and designer
  • Specialties: storage and storage interfaces
    • Current focus: flash memory and USB
  • Experienced with intellectual property and patents
  • Berg Software Design: www-bswd.com