Memory Modem™ FTL Architecture for 1Xnm / 2Xnm MLC and TLC NAND Flash

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Outline

• Requirements
• 1xnм/2xnм TLC NAND Flash Reliability Challenges
  • Reliability
    • BER Vs Endurance Vs Retention
    • Read / Program Disturbs
  • Integrity
    • “Ungraceful” power down
• DB3610 Memory Modem™ FTL Layered approach:
  • Lower Layer – Physical level reliability
  • Upper Layer – Memory management
Requirements

• Data Integrity and Reliability

• High Performance
  • Throughput
  • IOPs

• Low Power
  • Mobile devices
1xnm/2xnm Reliability Challenges (1)

• Bit Error Rate (BER) Vs Endurance Vs Retention:
1xnm/2xnm Reliability Challenges (2)

• BER Vs Endurance Vs Retention:
  • BER can go as high as 5e-2
  • Even without retention BER goes quickly up (1e-2)
  • 4x-5x factor in BERs due to retention

• ECC requirements
  • Near optimal reliability – close to theoretical bounds
  • Perform both hard and soft decoding
  • Optimal and high performance hard decoding
1xnm/2xnm Reliability Challenges (3)

- Retention effect:
  - Lobe widening
  - Lobe shift
1xn/m/2xn/m Reliability Challenges (4)

• Read Disturbs
1xn/m/2xn/m Integrity Challenges

• Power down scenarios
  • Managed power off
    • Required data-bases are stored prior to power down
  • Sudden power off between transactions (graceful power off)
    • All written data are recoverable through meta-data
  • Sudden power off within a write transaction (ungraceful power loss)
    • All data except for last (interrupted) transaction must be recovered
  • Past data may be damaged due to interruption
DensBits Memory Modem™ (1)

- DB3610 eMMC/SD Controller Functional Diagram
DB3610 Memory Modem™ (2)

- Memory Modem™ for Flash memories improving reliability, enabling smaller process nodes and more bits per cell
  - Proprietary ECC
  - Proprietary DSP
  - Proprietary Management
DB3610 Memory Modem™ (3)

- FTL Layered approach

![FTL Diagram]

- Higher Layer
  - Wear Leveling
  - Data Mapping
  - Bad Block handling

- Lower Layer
  - Virtual NAND dies
  - Virtual erase blocks
  - Virtual program pages
DB3610 Memory Modem™ (4)

• FTL Layered approach
  • Lower layer
    • Handles the data
    • Responsible for presenting a reliable virtual FLASH to the upper layer
  • Includes main parts of memory Modem™:
    – ECC flow
    – DSP software
    – Low-level memory management:
      » Data allocation
      » Damaged page recovery following “ungraceful” power-down
• FTL Layered approach
  • Upper Layer
    • Handles control data
    • Data mapping
    • Wear leveling
  • Data integrity issues:
    – Bad blocks handling
    – Power-down recovery – control data
    – Scrubbing
  • Metrics for lower layer to improve decisions
  • ....
DB3610 Memory Modem™ (6) - ECC

• Features
  • **Configurable**, input parameters (set via software):
    • Block size: 0.5KB-8KB
    • Code rate: 0.5 - 0.99
  • **Slim design / low power**
  • Hard and Soft decoding
  • Hard decoding as standard operation, soft decoding at extreme, **guaranteeing reliability with low latency**
  • Per each block size and code rate, **near-optimal error correction**
    • Near Hamming bound (hard decoding theoretical limit)
    • Near Shannon bound (soft decoding theoretical limit)
DensBits’ ECC – Hard Decoding

Theoretical limit (Hamming bound)

DensBits’ ECC - hard decoding

<table>
<thead>
<tr>
<th>Block [Bytes]</th>
<th>Spare [Bytes]</th>
<th>Coding rate</th>
</tr>
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<tbody>
<tr>
<td>8K</td>
<td>1445</td>
<td>0.85</td>
</tr>
<tr>
<td>8K</td>
<td>908</td>
<td>0.90</td>
</tr>
<tr>
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</tr>
<tr>
<td>8K</td>
<td>256</td>
<td>0.97</td>
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DensBits’ ECC – Soft Decoding

Theoretical limit (Shannon bound)

DensBits’ ECC - soft decoding
BCH(24, 1024)

0.8 0.82 0.84 0.86 0.88 0.9 0.92 0.94 0.96 0.98 1

10⁻⁴

10⁻³

10⁻²

10⁻¹

10⁰

Input BER achieving output BER < 10⁻¹⁵

Coding rate

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1Xnm MLC, TLC

2Xnm MLC, TLC
ECC FTL Flow

• Most common flow will perform hard decode
  • Enabled through hard decoding machinery
  • High performance

• Rare occasion, following retention, may require soft decoding
  • Performance price due to additional reads from flash memory
DB3610 Memory Modem™ (7) - DSP

• Optimized read parameters
  • Optimization of read parameters minimizing the input BER for the ECC
  • “Blind” threshold acquisition
  • Optimization of performance through:
    • Block-state tracking
    • Continuous block state updates
• Optimization of program parameters, depending on block state, minimizing tPROG
DSP FTL Flow

- Read Flow:
• Different page types may have different reliability:
  • Even / Odd pages
  • MSB / CSB / LSB pages

• Data allocation can significantly improve data reliability:
  • Striping / Interleaving
  • Variable rate coding
  • BER equalization
  • X2 improvement in BER
DB3610 Memory Modem™ (9)

• Upper Layer – Data Mapping
  • Hybrid block/page level mapping
    • High IOPs
    • Low WA
    • Can be accommodated in an embedded system
• Wear leveling
• Other reliability considerations:
  • SLC block allocation
Summary

• 1xnm / 2xnm NAND Flash controllers require a Memory Modem™ to obtain full reliability and performance
• A layered approach is a useful abstraction allowing handling various Failure mechanisms
The Future of NAND Flash Technology

Extreme Reliability, Unparalleled Performance
Thank You!