ECC/DSP System Architecture for Enabling Reliability Scaling in Sub-20nm NAND

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August 2013
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Disclaimer: This tutorial provides an overview of various techniques and concepts, some or all of which may not necessarily reflect what SanDisk is actually using in their products.
Outline

- Gap Between Product Requirements and Technology Capability
  - Applications Requirements: Endurance, Performance, Power
  - Reliability Challenges with Scaling

- ECC/DSP solutions
  - Tier 0: Adaptive NAND Parameters Optimization
  - Tier 1: Noise Reduction
  - Tier 2: Advanced Error Correction Coding (ECC)
  - Tier 3: Second level Error Correction (RAID)
  - Tier 4: Flash Management Algorithms
  - Tier 5: Host Data Manipulation

- Summary

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Increasing Product Requirements

- Faster Application Execution
- Faster Web Browsing
- Smoother Multi-tasking
- Computational Photography
- Longer Battery Life, Power Savings
- Sharing, Connectivity
- Higher Resolution Video

SanDisk
Gap Between Raw Memory Capability and Applications Requirements
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AFM 4.0 Multi-dimensional Adaptive Flash Management™ Technology

AFM 1.0 Performance Leadership
AFM 2.0 Application Awareness
INAND™ EFD “Classic”

Email, Music, & Video
Multitasking Apps
 Computing

56nm 43nm 32nm 24nm 19nm 1Ynm 12nm
Reliability Degrades
Performance Deteriorates

Cost Reduction

Lower Power Consumption
Better Performance
Higher Endurance

SanDisk
Optimized **Endurance** for enhanced video download & application caching
Optimized Performance for superior gaming experience

Better Performance

Lower Power Consumption

Higher Endurance
Optimized Power Consumption for longer web browsing

Lower Power Consumption
Reliability Challenges with Scaling

As an example we will describe the phenomena of Read Disturb
Read Operation

1. BL Pre-Charge
**Read Operation**

*Threshold Voltage numbers are nominal*

1. BL Pre-Charge
   - Opens “select gate” transistors
2. Gate Voltages
   - Opens unselected cells – “Victims”
   - Senses state of selected cell – “Target”
Read Operation

**Target Cell is Erased – Read “1”**

1. BL Pre-Charge
2. Gate Voltages
3. Sensing
Read Operation

Target Cell is Erased – Read “1”

1. BL Pre-Charge
2. Gate Voltages
3. Sensing
Read Operation

Target Cell is Erased – Read “1”

1. BL Pre-Charge
2. Gate Voltages
3. Sensing
Read Operation

Erased Cell – Read “1”

1. BL Pre-Charge
2. Gate Voltages
3. Sensing

Current is Sensed
➢ Cell is Erased!
Read “1”
Read Operation

Target cell is Programmed – Read “0”

1. BL Pre-Charge
2. Gate Voltages
3. Sensing

Current is NOT Sensed

➢ Cell is Programmed!
Read “0”
Read Disturb

Er → A
Read Disturb

- P/E cycles leads to Tunnel Oxide (Tox) degradation that creates traps
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“Weak Programming” in unselected cells due to unintentional tunneling of electrons to the FG
Read Disturb

- P/E cycles lead to Tunnel Oxide (Tox) degradation that creates traps
- “Weak Programming” in unselected cells due to unintentional tunneling of electrons to the FG
ECC/DSP Methods: from NAND to System

- Adaptive NAND Parameters Optimization
- Noise Reduction
- Advanced Error Correction Coding (ECC)
- Second level Error Correction (RAID)
- Flash Management Algorithms
- Host Data Manipulation
Error Handling System Solutions

Early Technologies

ECC
Error Correction Coding (BCH)

1e-21 Few Errors

1e-1 Many Errors

Basic ECC sufficient to meet application requirements
Sophisticated ECC and DSP techniques applied to mitigate the natural drift in reliability, and to meet the more demanding requirements of embedded application.
Tier 0: Adaptive NAND Parameters Optimization

- Adaptive NAND parameters optimization along the memory lifetime.
- Parameter setting (“trimming”) of the Program, Erase and Read parameters.
- System level feedback adapts the parameters to:
  - Memory wearing and error rates along the lifetime
  - Die to die, block to block, WL to WL variations within the memory
  - Host data patterns
- Once NAND level optimization has been exhausted, the residual noises and errors need to be handled at system level
Adaptive Read Thresholds – Example

Problem:
- Cell Voltage Distribution is not fixed:
  - Changes along the memory lifetime with W/E cycling and time (DR)
  - Variations within a die - changes from Block to Block, WL to WL,…
- Using a fixed set default thresholds result in high BER and decoding failure

Solution:
- Adaptive read thresholds
Tier 1: Noise Reduction

- System level residual NAND “noise” reduction via DSP and coding techniques, aimed at reducing error rates to a bare minimum level
  - Tier 1 countermeasures may reduce raw NAND error rates from a ~1E-1 error level to ~1E-2 error level
  - Tier 1 countermeasures are aimed at:
    - Ensuring that the next Tier 2 Error Correction Coding (ECC) is cost effective (i.e. less redundancy)
    - Maximizing performance and reducing power consumption
  - Tier 1 countermeasures deal with non intrinsic “noises”, which can be cancelled out, mitigated or compensated for:
    - Data dependent noises such as cross-coupling induced widening, back pattern effects, Program and Read Disturbs, Over programming errors, etc.
NAND Scaling Challenges – Interferences

Source: Semiconductor Insights
Cross Coupling Widening effect
Cell-to-Cell Coupling (CCC) Trend

- With technology scaling, CCC increases dramatically
- Air Gap technology make the 19nm (AG) CCC equivalent to 24nm (no AG)~ 27% reduction
Mitigating Data Dependent Noises

Digitally mitigating cross coupling and other data depended noises during read by taking into account the neighboring cell’s read state.

Example: Read LSB page

Without utilizing neighbor cell information:
LSBit = “0” with low reliability

With utilizing neighbor cell information:
LSBit = “1” with high reliability
Tier 2: Advanced Error Correction Coding (ECC)

- Advanced Error Correction Coding (ECC) is required in order to handle the residual errors of tier 1
  - Tier 2 ECC can reduce the ~1E-2 residual error levels of tier 1 to ~1E-16 error level
  - State of the art iterative coding techniques, such as LDPC, are replacing algebraic coding techniques, such as BCH codes
  - Advanced ECC techniques are essential for achieving an optimal cost, endurance and performance tradeoff, as they allow operation near the theoretic limits (Shannon limit), providing maximal correction capability for a given amount of overprovisioning (“ECC redundancy”)
How can we compute the Flash capacity?:  Information Theory (Shannon 1948)

Based on knowing probability to read a voltage level $Y$ given that a voltage level $X$ was programmed.

For such a simplified model:

\[
C = \max_{P(X)} I(X;Y) = \max_{P(X)} \sum_{X,Y} P(X)P(Y | X) \log_2 \left( \frac{P(Y | X)}{\sum_X P(X)P(Y | X)} \right) \] information bits

\[
\frac{\text{cell}}{}
\]

Actual computations are more complicated. Depend on:

- Verify and read voltage levels
- Data retention
- P/E cycles
- Temperature
- Tuning voltage ambiguity
- Cross coupling
- Back pattern
- Program/Read disturb
- …
Approaching the Shannon Limit

Source: Forward Insights
Tier 3: Second level Error Correction (RAID)

- For enhanced reliability, especially required for SSD applications, a second level error correction, aimed to deal with complete NAND failures resulting in colossal errors, is required. RAID like techniques are used for that purpose.
  - Tier 3 level protection is used for both:
    - Reducing tier 2 error rates from \( \sim 1 \times 10^{-16} \) to \( \sim 1 \times 10^{-24} \) or lower
    - Reducing dPPM levels due to gross NAND failure, such as WL breaks, WL shorts, etc.
  - Tier 3 protection may require extra overprovisioning, or may only maintain the overprovisioning temporarily in the controller until verifying data integrity.
RAID Example
Tier 4: Flash Management Algorithms

- Back End Flash Management algorithms which manage how logical data is stored on the physical NAND level, in a way that will provide the best performance (both sequential, random or any other combined use case) and the best endurance

- Examples of Flash management functions are:
  - Logical to physical address
  - Wear leveling
  - Garbage collection
Host data manipulation, leveraging the inherent “redundancy” in the host data for improving endurance, performance and power

- Examination of host data produced by users or arising from various operating and file system shows that a significant fraction of the data is of low entropy, having many repetitive data patterns
- Low entropy data from the host can be manipulated by the controller in various ways:
  - Compression, Endurance coding, Deduplication
Summary

Optimization for Endurance

Tier 0:
Adaptive Parameters

Tier 1:
Noise Reduction

Tier 2:
Advanced ECC

Tier 3:
Second Level Error Correction

Tier 4:
Flash Management Algorithm

Tier 5:
Host Data Manipulation

Optimization:
Optimization for different tradeoffs

Optimization for Power

Lower Power Consumption

Higher Endurance

Better Performance

Flash Memory Summit

SanDisk
Thank you!