Extending Flash Memory Through Adaptive Parameter Tuning

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Take Home Messages

- 25x increase in endurance on 1X nm devices
  - Machine learning software fully characterizes NAND chips before they go into a product
  - Lightweight software running on the product autonomically manages its health, using machine learning knowledge
  - 40-bit ECC gives 10x increase; 120-bit ECC gives 25x increase
- Uses the least *stress* possible
- Raw flash runs *faster*
At a glance

- **NVNdurance Pathfinder**
  - Delivers most of the endurance gain
  - Suite of Machine Learning Algorithms
  - Determines sets of optimal register values for NAND chips before they go into a product
  - “Heavy lifting” done before shipping

- **NVNdurance Navigator**
  - Exploits endurance gains enabled by Pathfinder
  - Autonomic system, runs on the controller
  - Chooses register values at run-time from those discovered by Pathfinder
The Problem

Stress applied at Time X

It’s easier to pass retention tests with less cycling done…
… but flash chips use the same write register values throughout their lifetime!

Number of P/E Cycles

Stress

Pass after 3K cycles

Pass after 1K cycles
Solution

Vary stress over time

- Pass after 5K cycles
- Pass after 10K cycles
- Pass after 20K cycles
- Pass after 30K cycles
Solution

- Which registers to change?
- What values to change to?
- When to make the changes?

Each register adds two dimensions of search

Number of P/E Cycles
Solution

Stress

Vary stress over time

Number of P/E Cycles

Pass after 5K cycles
Pass after 20K cycles
Pass after 30K cycles
Pass after 10K cycles
Pass after 5K cycles
Solution with variable ECC

Vary stress over time, spend more time at each level

- Pass after 10K cycles
- Pass after 20K cycles
- Pass after 30K cycles
- Pass after 60K cycles

Number of P/E Cycles
Solution with variable ECC

Which registers to change?
What values to change to?
When to make the changes?
How much ECC to use?

Number of P/E Cycles

Pass after 10K cycles
Pass after 20K cycles
Pass after 30K cycles
Pass after 60K cycles
The Not-So-Secret Sauce

- Reduce dimensionality of the problem
  - Reduce the number of independent variables
  - Understand the silicon; vary as few registers as possible

- Guide the search
  - Be sensible, if not insightful

- Test only what has to be tested
  - Or at least know what NOT to test

...this is still an astronomically difficult problem!
The Secret Sauce

- Plot “safe” paths through massively highly dimensional space
  - Each register adds two dimensions (more than 50 write registers!)
- Tune paths on the fly
  - Not all blocks degrade at the same rate
  - Retention may impact various blocks differently
  - Anticipate health issues before they happen
- Treat the flash as though it is a dynamic, living thing
Imagine the lifetime of a device to be a journey through space...
... touch an “asteroid” and we have unrecoverable data
NVMduration Pathfinder

Start

Destination
NVMdurance Pathfinder

Start

Destination
NVMdurance Pathfinder
NVMdurance Pathfinder

Start

Destination

... and beyond!
NVMdurance Pathfinder

Start

Destination
NVMdurance Pathfinder

Start

Destination
NVMdurance Pathfinder

Start

Destination
NVMdurance Pathfinder
NVMdurance Pathfinder determines sets of optimal register values (analogous to safe paths through the asteroid belt) for NAND chips before they go into a product.
NVMdurance Navigator

Asteroid Belt

Live on device, NVMdurance Navigator chooses which path through the space to use, based on the “health” of the device.
Live on device, NVMdurance Navigator chooses which path through the space to use, based on the “health” of the device.
NVMduration Navigator

Start

Asteroid Belt

Destination

Hit the *hyperspace button*! Change the register values
NVMduration Navigator constantly monitors the health, and jumps and jumps from path to path as the use-case requires.
NVMdurance Navigator constantly monitors the health, and jumps and jumps from path to path as the use-case requires.
NVMdurance Navigator constantly monitors the health, and jumps and jumps from path to path as the use-case requires.
Asteroid Belt

NVMdurance Navigator constantly monitors the health, and jumps and jumps from path to path as the use-case requires.
NVMdurance system

Machine Learning Parameter Discovery

*NVMdurance Pathfinder*: Discover routes through multidimensional space such that every parameter set passes retention for that point of life (by fully characterizing NAND chips before they go into a product).

Autonomic (runs live on the SSD controller)

*NVMdurance Navigator*: Observes deterioration of the SSD; chooses when to change parameters (using the knowledge delivered by Pathfinder).
Sets of **Write register values** for that time in life

- 30-60 write registers, e.g. start voltage, step size, MSB, LSB, odd, even, etc.
- More registers means more control, but larger search space
Sets of **Write register values** for that time in life

- 30-60 write registers, e.g. start voltage, step size, MSB, LSB, odd, even, etc.
Stage

- Each stage has multiple waypoints (each a set of read register values) to guide it to the next stage
  - Often only one set in early life - no read retry!
  - First stage often lasts longer than default!
  - Never more than eight waypoints
Waypoints

- More waypoints required later in life
  - Higher wear uncovers higher variability
Lifetime

- NVMdurance Pathfinder (machine learning offline)
  - Automatically discovers and proves viability of stages
  - Each stage passes retention test

P/E Cycle Count as Multiple of Default Rating
Lifetime

- NVMdurance Navigator (run time)
  - Runs on controller (autonomic)
  - Monitors “Health” of devices
  - Determines when to progress to next stage
  - Chooses which waypoint to use during each stage

P/E Cycle Count as Multiple of Default Rating
Increasing ECC

- System can tolerate higher BER
  - Stages last longer
  - Weaker stages possible earlier in life
  - NVMdurance enables a truly variable/adaptive ECC

P/E Cycle Count as Multiple of Default Rating
One approach - many use cases

P/E Cycle Count as Multiple of Default Rating (40-bit ECC)

P/E Cycle Count as Multiple of Default Rating (120-bit ECC)
## Target Device

<table>
<thead>
<tr>
<th>Device</th>
<th>1X nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECC</td>
<td>Up to 40 bits per sector</td>
</tr>
<tr>
<td>Retention</td>
<td>12 months</td>
</tr>
<tr>
<td>Baseline Endurance</td>
<td>1</td>
</tr>
<tr>
<td>Intrinsic Endurance (3 months retention)</td>
<td>1.8x longer than rated endurance</td>
</tr>
</tbody>
</table>
### Summary

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
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<tbody>
<tr>
<td><strong>Number of stages</strong></td>
<td>8</td>
</tr>
<tr>
<td><strong>Stage length</strong></td>
<td>1x - 2x longer than rated endurance</td>
</tr>
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<td><strong>ECC</strong></td>
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<tr>
<td><strong>Minimum Window Stress (stage 1)</strong></td>
<td>45%</td>
</tr>
<tr>
<td><strong>Approximately equal stress</strong></td>
<td>Stage 5</td>
</tr>
<tr>
<td><strong>Maximum Window Stress (stage 8)</strong></td>
<td>120%</td>
</tr>
<tr>
<td><strong>Maximum P/E cycles</strong></td>
<td>10x longer than rated endurance</td>
</tr>
</tbody>
</table>
Results

P/E Cycle Time & Write Stress Vs P/E Cycles

- Normal End of Life
- Extended endurance with NVMdurance (40 bit ECC)

P/E Cycle Time as % of Default

Write Stress as % of Default

P/E Cycle Count as Multiple of Default/Rating

- Blue: P/E Cycle Time
- Red: Write Stress
Results

P/E Cycle Time & Write Stress Vs P/E Cycles

Extended endurance with NVMdurance (40 bit ECC)

Default lifetime, normalized to one
Initial write stress starts at 45% of default
Write stress slowly increases.

Extended endurance with NVMdurance (40 bit ECC)
Results

P/E Cycle Time & Write Stress Vs P/E Cycles

- Normal End of Life
- Extended endurance with NVMdurance (40 bit ECC)

Write stress exceeds default level
Results

P/E Cycle Time & Write Stress Vs P/E Cycles

Extended endurance with NVMdurance (40 bit ECC)

10x increase in endurance
Results

P/E cycle time as % of default; never exceeds default.

P/E Cycle Time & Write Stress Vs P/E Cycles

P/E Cycle Time as % of Default

Write Stress as % of Default

P/E Cycle Count as Multiple of Default/Rating

Extended endurance with NVMdurance (40 bit ECC)

Normal End of Life
Results - Increasing ECC

Stages get longer as ECC increases.
Results - Increasing ECC

Stages get longer as ECC increases.
Results - Increasing ECC

Stages get longer as ECC increases
Results - Increasing ECC

Stages get longer as ECC increases.

P/E Cycle Time & Write Stress Vs P/E Cycles

- P/E Cycle Time
- Write Stress

Normal End of Life

P/E Cycle Count as Multiple of Default/Rating

Write Stress as % of Default

P/E Cycle Time as % of Default
Results - Increasing ECC

Stages get longer as ECC increases.
Results - Increasing ECC

25x improvement in endurance with the same retention!
Results

P/E Cycle Time & Write Stress Vs P/E Cycles

- Normal End of Life
- Extended endurance with NVMdurance (40 bit ECC) (120 bit ECC)

Initial write stress starts at 25% of default
Results

P/E Cycle Time & Write Stress Vs P/E Cycles

Write stress increases more slowly
**Results**

P/E Cycle Time & Write Stress Vs P/E Cycles

- **Extended endurance with NVMdurance**
  - (40 bit ECC)
  - (120 bit ECC)

Write stress exceeds default level

Flash Memory

nvm_durance

Write stress exceeds default level
P/E cycle time as % of default; never exceeds default.
### Results

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Results Summary

- 25-fold increase in endurance on 1X nm
  - 10-fold increase on 1X with 40-bit ECC
- We avoid the problem of live optimization of parameters
  - Most work done before flash is put in product
- NVMdurance Navigator can predict imminent failure
  - Our “health” measure is very precise
- P/E operations run faster than defaults
- Results proven with current generation devices from multiple manufacturers
Conclusion

- Industry leading endurance gains
- NVMdurance's technology is synergistic to existing flash controller technology
  - Machine-learning software fully characterizes NAND chips before they go into a product
  - Lightweight software running on the product autonomically manages its health, using that knowledge

Stop by and see us at booth #921
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