Reliability Tradeoffs For Flash-Based Error Correction

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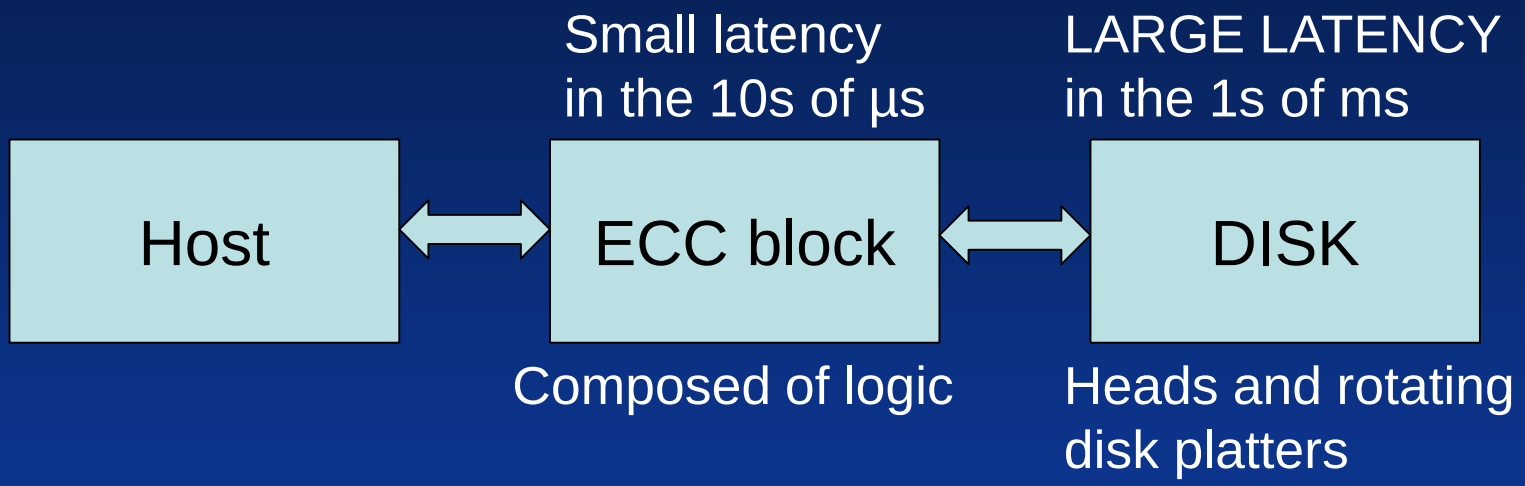
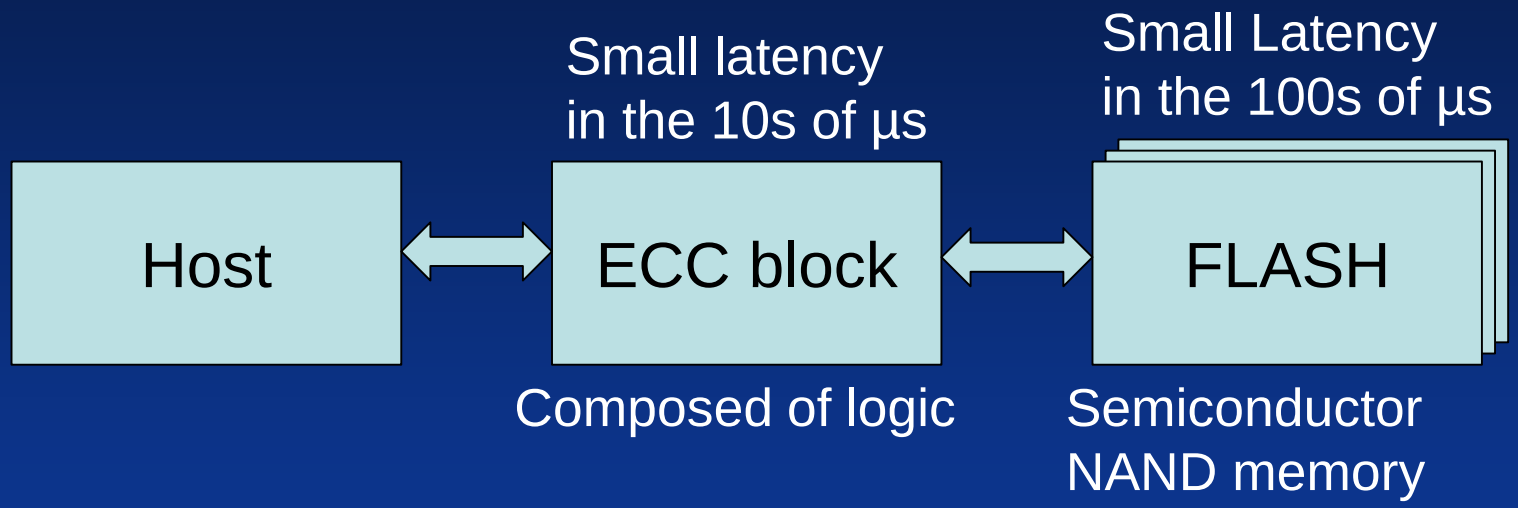
Presentation synopsis

- The presentation will address the tradeoffs in choosing between BCH and LDPC error correction methodologies in flash-based storage. Included will be a discussion of the compiler technology necessary to implement LDPC as compared with BCH, how it affects flash reliability, and how it is implemented for ASIC, FPGA and eASIC devices.

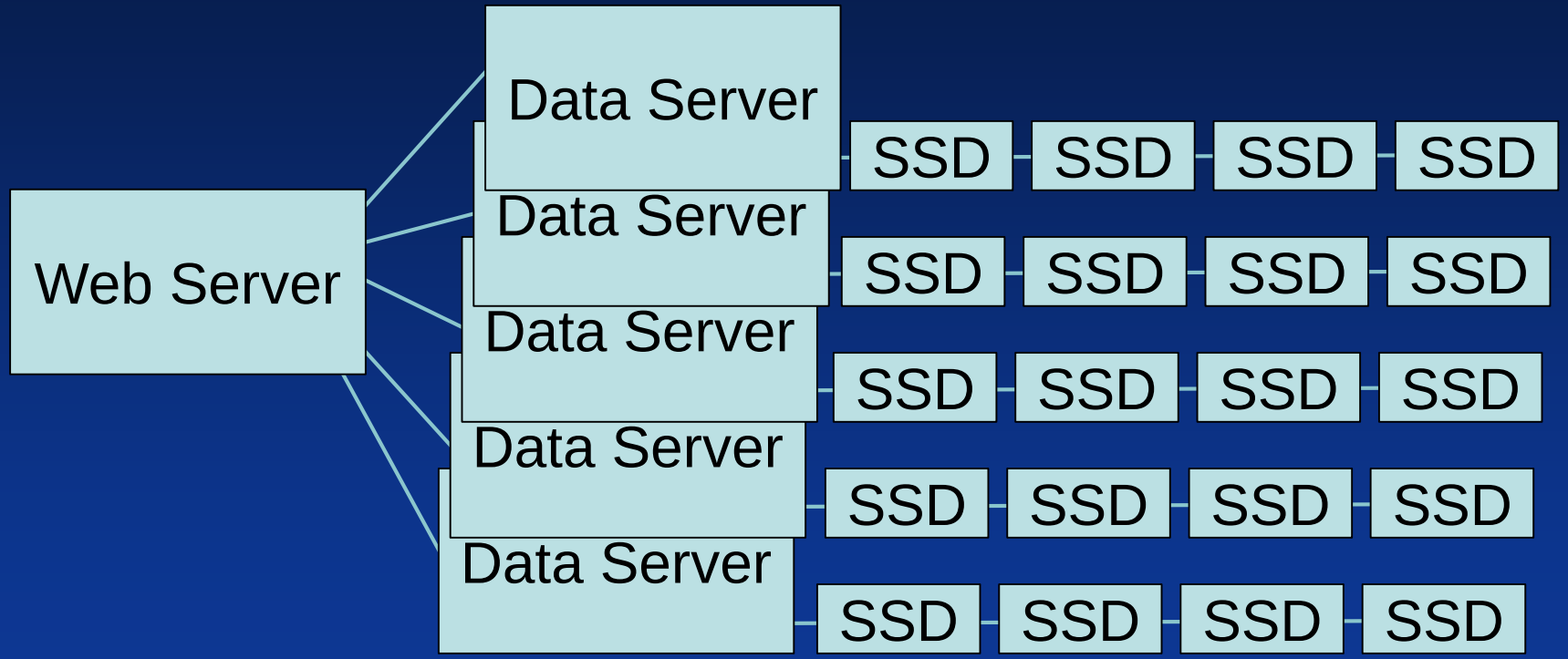
Background: ECC with HDD



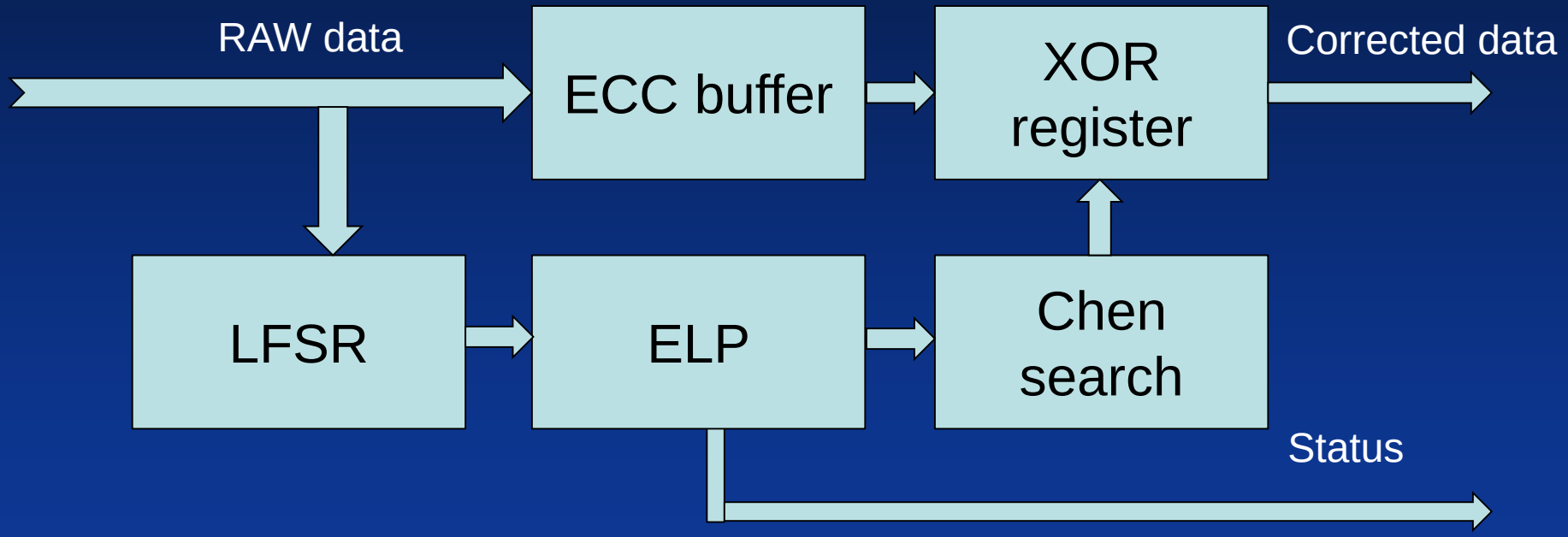
Background(2): ECC with flash



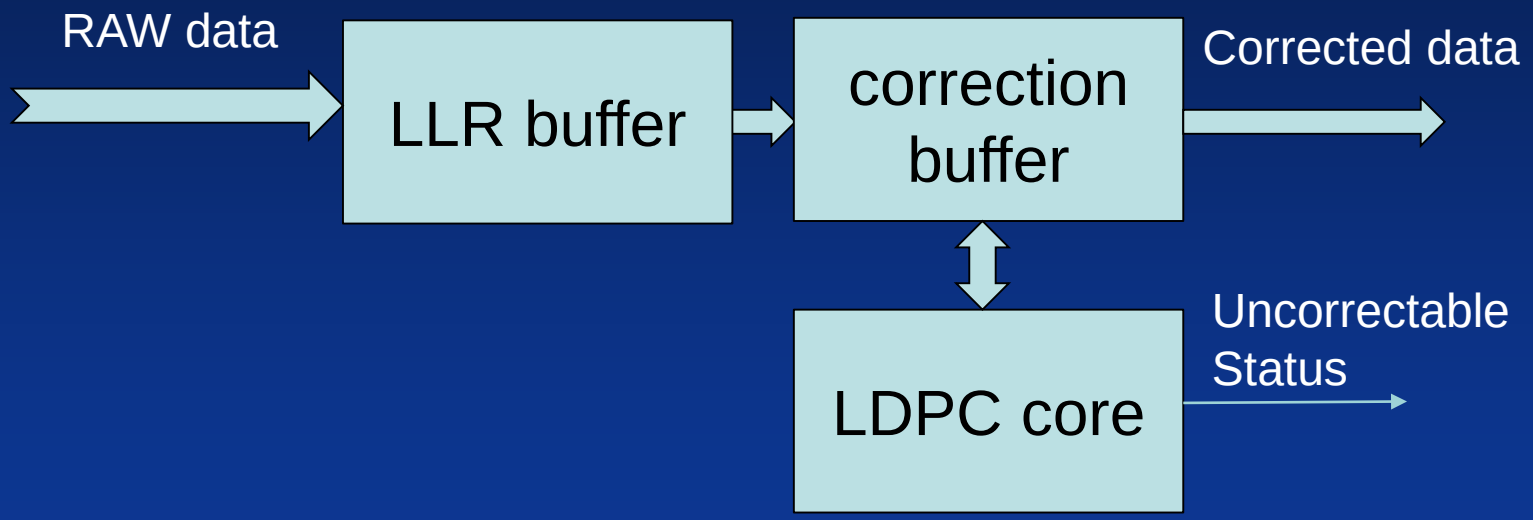
Tail Latency (Latency at Scale)



Attributes of BCH



Attributes of LDPC



Compliers and configurability

- LDPC and BCH can be compiled to fit requirements.
- LDPC for H and G matrix's are stored in SRAM to perform various sizes and levels of correction based upon needs.
- BCH can be compiled to fit many requirements for storage including number of errors of correction and root polynomial including the speed of correction.
- Data path width's and clock speed can be configured.

Attributes of flash

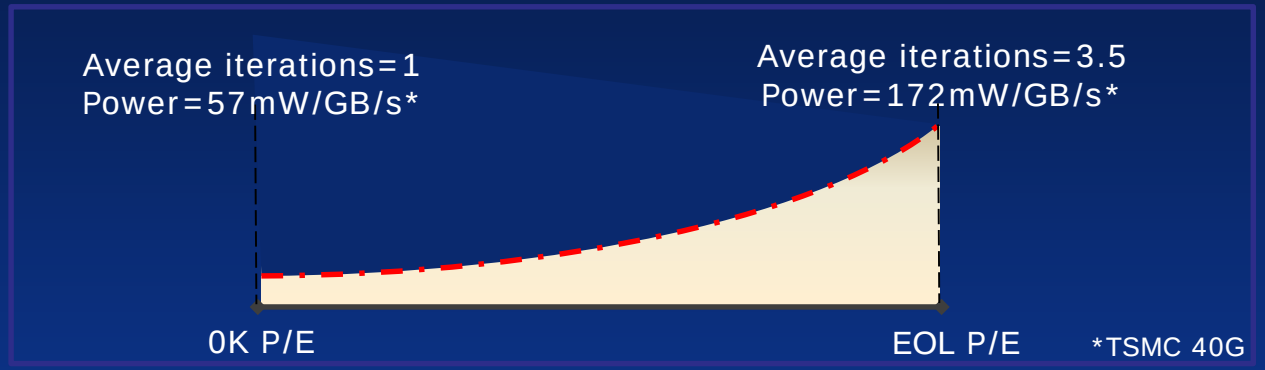
Type A	Type B	Type C
Even Page 30 Bits	Page X 30 Bits	Page 0-50 30 Bits
Odd Page 60 Bits	Page Y 45 Bits	Page 50-200 45 Bits
	Page Z 60 Bits	Page 200-256 60 Bits

Implementation choices

- With a requirement of latency
  - BCH if gate count is do-able
  - LDPC with hard decision decoding in normal operation
- More flexible latency profile
  - BCH if gate count less than LDPC implementation
  - LDPC with hard/soft decision decoding

Sufficient Iterations for end of life

- LDPC decoder computational load and power consumption increase towards the end-of-life of SSD:



- Mobiveil's LDPC guarantees sufficient iterations for end-of-life
  - Guaranteed sustained LDPC iterations per code word at the end of life:
  - 3.5 average iterations for column weight=3
  - 2.8 average iterations for column weight=4
  - Maximum iteration limit is programmable and is typically much higher (e.g. 8-30)
- Data-rates quoted are for end-of-life operation (average sustained iterations as above, no sector gaps)

Mobiveil LDPC compiler

- LDPC scalable platform
  - Supporting a wide range of data-rates
  - 50MB/s to 4.0GB/s for a single LDPC instance
  - IP has been ported to FPGA, eASIC and ASIC (40LP UMC, 40G and 28HPM TSMC)

- Major scalability parameters are:
  - Codeword size (0.5KB vs. 1KB vs. 2KB, etc.)
  - Maximum amount of supported parity
  - Several parameters for degree of parallelism
  - Memory access options

- All LDPC IP Cores share the following features:
  - Simultaneous support for different amounts of parity
  - Simultaneous support for several LDPC codes
  - On-the-fly switching from one LDPC code to another
  - Low area and power

Design Implementation of IP

- Support ASIC, eASIC and FPGA implementation and integration

- ASIC implementation
  - Design had been instantiated in TSMC (28 and 40nm) and UMC (40nm)
  - Support for customer design environment and libraries

- eASIC implementation
  - LDPC design optimized for eASIC (structured ASIC)
  - Full integration with eASIC design flow

- FPGA implementation
  - LDPC design optimized for FPGA (additional options)

LDPC IP Deliverables

- Complete reference design for Flash Reliability System Solution
  - Architecture SW tools
  - Digital IP Core
  - Firmware routines
  - FPGA prototype
  - Software suite for data analysis

Questions?

- Thank you